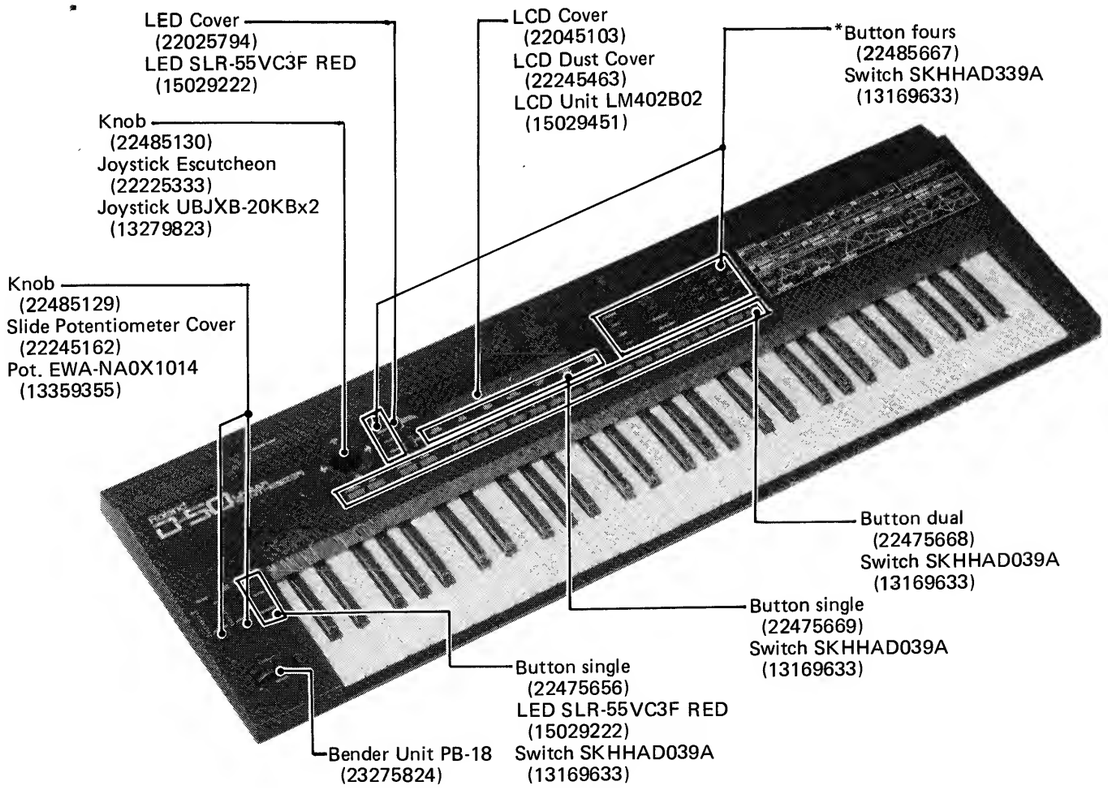
D-50

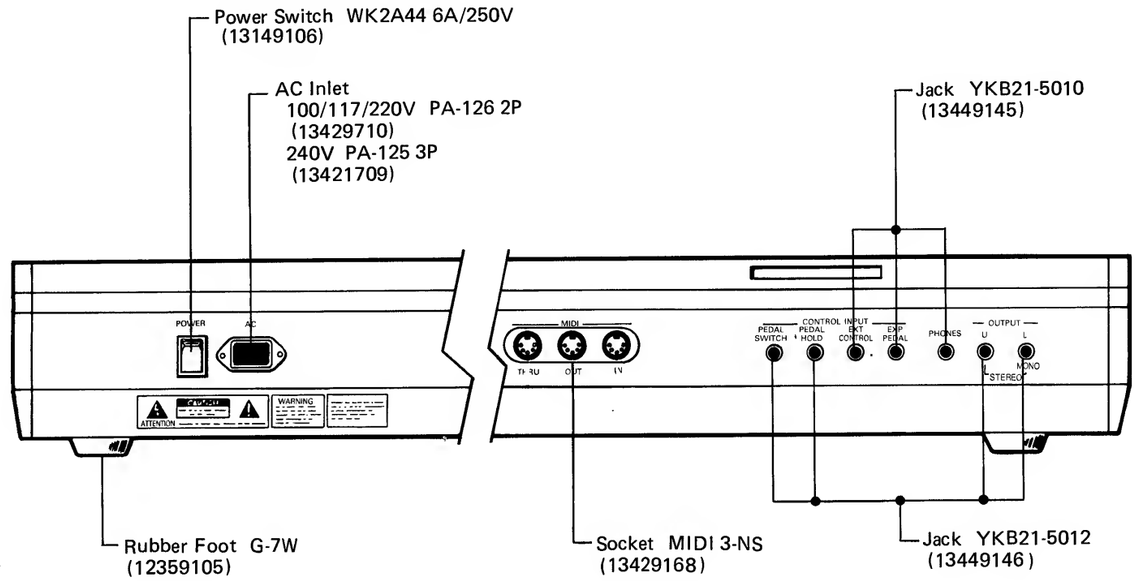
SERVICE NOTES

First Edition

SPECIFICATIONS

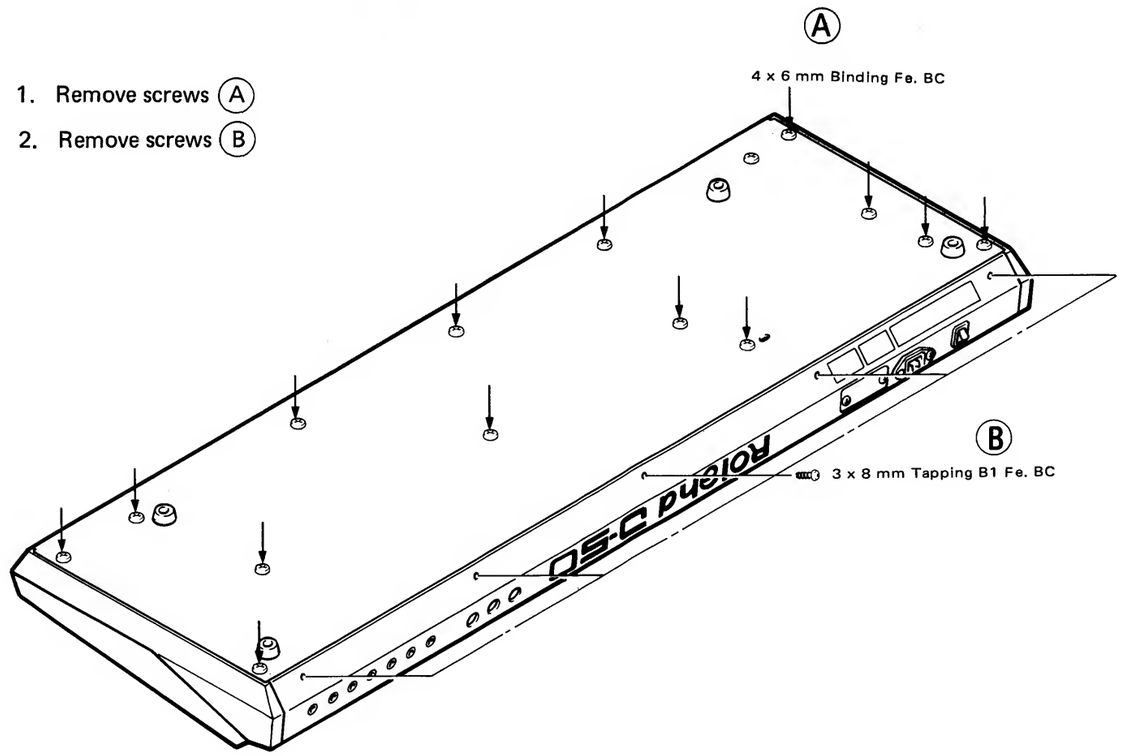
KEYBOARD	61 key, 5 octave, C scale with Velocity and Aftertouch	
TUNE	MASTER TUNE	±50 cents
	FINE TUNE	±50 cents
PITCH MODULATION	LFO	±600 cents
	ENV	±2400 cents
	BENDER	±2400 cents
	AFTERTOUCH	±2400 cents
ENV TIME	PITCH T1 – T4	9ms – 9s
	TVF T1 – T5	4ms – 80s
	TVA T1 – T5	4ms – 80s
LFO	RATE	0.0004 – 27Hz
	DELAY TIME	0 – 10s
CHORUS LFO	RATE	0.098 – 20Hz
OUTPUT	AUDIO	–4.0dBm
	PHONES	8 – 150Ω Stereo
POWER CONSUMPTION	22W, 15W (Japan)	
DIMENSIONS	974(W) x 332(D) x 94(H) mm	
	38-3/8" x 13-1/6" x 3-11/16"	
WEIGHT	10.5 kg/23 lb 2 oz	
ACCESSORY	MEMORY CARD (ROM) PN-D50-00 (12379401)	





DISASSEMBLING/分解手順

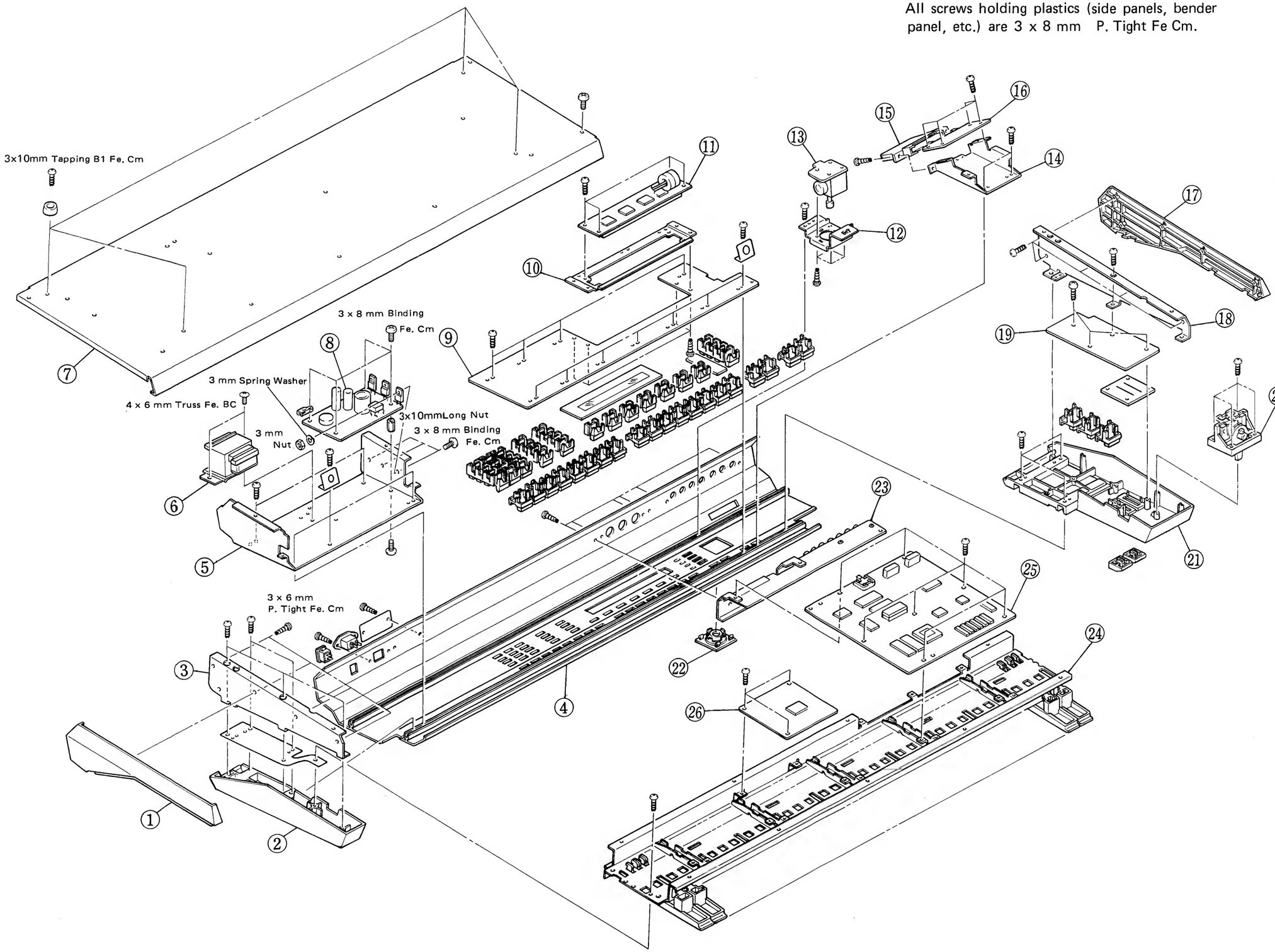
1. Remove screws (A)
2. Remove screws (B)



EXPLODED VIEW／分解図

Unless otherwise noted:
All screws holding metal parts are 3 x 8 mm tapping B1 Fe Cm.
All screws holding plastics (side panels, bender panel, etc.) are 3 x 8 mm P. Tight Fe Cm.

図中に指示なきビスの名称は，次の通りです。
・パネルやホルダー等の金属に止めるビス類は全て3×8mm Tapping B1 Fe Cm
・側板やベンダー・パネル等のプラスチックに止めるビス類は全て3×8mm P.TIGHT Fe Cm



No.	PART NAME	PART No.
1	Lower Side Panel R	21125282
2	Side Panel R	22215783
3	Side Holder R	22195956
4	Front Panel	22215546
5	Transformer Holder	22195950
6	Power Transformer universal	22455480U0
7	Bottom Case	22815588
8	Power Supply Board Assy 100 ／ 117V 220 ／ 240V	76180161 76180164
9	Panel Board Assy	76180120
10	LCD Holder	22195952
11	LCD Unit(LM402B02)	15029451
12	Joystick Holder	22195953
13	Joystick Board Assy	76180140
14	Card Slot Holder	22195925
15	Card Holder	22195954
16	Memory Card Board Assy	76180130
17	Lower Side Panel L	21125281
18	Side Holder L	22195955
19	Bender Board Assy	76180110
20	Bender Unit PB-18	23275824
21	Bender Panel	22215784
22	Joystick Escutcheon	22225333
23	Jack Board Assy	76180100
24	Keyboard SK-361-PW	76180200
25	Main Board Assy	76180090
26	Dyna scan Board Assy	76180161

PARTS LIST

Excluded in this list are the chip components attached to the rear side of Bender, and Jack and Dyna scan boards with a thermo-setting adhesive. These components won't separate by the conventional desoldering method.
Alternatively, some of them can be replaced by transitional ones: Isolating them by first cutting the foil patterns and soldering the replacement across the patterns. For these components consult local Roland service representatives. Chip components on the part side of Main board are replaceable.
Components such as resistors and capacitors not listed in this list are recommendably replaced by locally available ones in the mannar as described above.

チップ部品について
交換可能な部品以外は，パーツ・リストから除外しています。
交換の際は，下記の処置を行って下さい。
・ベンダー・ボード，ジャック・ボードやダイナスキャン・ボードのパターン面のチップ部品は，接着されているため取り外すことができません。したがってICや抵抗アレイなどの交換の際は，基板交換となります。ただし，抵抗，コンデンサーやダイオードなどは，チップ部品の両端をパターン・カットした後，通常のパーツで代用してください。
・メイン・ボードの部品面にハンダ付けされているチップ部品は，取り外すことができますが，特殊なチップ部品を除き通常のパーツで代用してください。

CASING

22215546	Front Panel	
22215783	Side Panel R	
22215784	Bender Panel	
22025794	LED Cover	
22045103	LCD Cover	
22245463	LCD Dust Cover	
22245162	Slide Potentiometer Cover	
22225333	Joy Stick Escutcheon	
21125281	Lower Side Panel L	
21125282	Lower Side Panel R	
22815588	Bottom Case	
12359105	Rubber Foot G-7W	

BUTTON/KNOB

22485130	Knob	joy stick
22485129	Knob	VOLUME
22475669	Button (single)	AFTERTOUCH
22475667	*Button	KEY MODE, etc.
22475668	Button (dual)	0, 2, 5, 8 (set), etc.
22475656	Button (single) With LED window	PATCH BANK, etc. KEY TRANSPOSE CHASE PORTAMENT

**This type separable into four: replacement single type only.*
このボタンは4つに分割可能。したがって，補修品はシングルで供給します。

KEYBOARD

76180200	SK-361-PW	61 key

**See KEYBOARD PARTS LIST for details.;*
詳細は鍵盤パーツ・リスト参照。

AC COAD SET (Detachable)

13439825	DC-320-J01	100V
13439812F0	UC-704-J01	117V
13439813F0	EC-210-J06	220V
13439846	BH-301-J0f1	240V England
13439814F0	SC-415-J06	240V Australian

SOCKET

13429710	PA-126 2P AC Inlet	100/117/220V
13421709	PA-125 3P AC Inlet	240V
13429168	MIDI 3-NS (triplet)	MIDI IN/OUT/THRU
13449145	YKB21-5010 (stereo)	PHONES, EXP PEDAL, EXT CONTROL
13449146	YKB21-5012 (mono)	OUTPUT (U/L), PEDAL SW, PEDAL HOLD
13429534	ICE-286-S-TG	EP-ROM

SWITCH

13169633	SKHHAD039A	bender board panel board
13149108	WK2A44 6A/250V	power switch

FUSE

12559411	SD6 315MA	100/117V
12559380	SD6 1.25A-N1	100/117V
12559540	CEE-160MAT BESWICK	220/240V
12559549	CEE-1.25AT BESWICK	220/240V

POWER TRANSFORMER

22455480U0	Power universal	100/117/220/240V

BENDER UNIT

23275824	PB-18	
	PB-18 is the same as PB-13, PB-14. Difference is wiring system only. When substituting with another type, be sure to reconnecting lead wirers.	
	PB-18は，PB-13，PB-14とユニット本体は同じです(ワイヤリング，コネクターは異なる)。代用する場合は，コネクターピンの配置を確認の上，ワイヤリングをつなぎかえてください。	

LCD UNIT

15029451	LM402B02 with EL, PCB and wirings	
	No replacement for individual parts.	
	補修品はユニット単位	

PCB ASSEMBLY

76180090	Main Board (PCB 22925445)	
	**Check PROM and CPU for reversion number by referring to CHANGE INFORMATION. Specify them when ordering. (Incompatible problem might occur.)*	
	メイン・ボードを発注の際は，変更案内を参照の上，CPUおよびPROMのバージョンを確認し，必要なバージョンを明記して下さい(バージョンによっては互換性がありません)。	
76180100	Jack Board (PCB 22925446)	
76180110	Bender Board (PCB 22925446)	
76180120	Panel Board (PCB 22925448)	
76180130	Memory Card Board (PCB 22925448)	
76180140	Joy Stick Board (PCB 22925448)	
76180150	Dyna Scan Board (PCB 22925449)	
76180161	Power Supply Board 100/117V (PCB 22925447)	
76180164	Power Supply Board 220/240V (PCB 22925447)	

**Difference between versions: Only in fuse system. Any version can be supplied as a replacement for particular voltage order, with correct fuses. Specify the line voltage when ordering.*
電圧による違いはヒューズの値のみで，補修用には異なった電圧のものが供給されることもあります。この際は，ヒューズが適当な値のものに取り替えられているか確認してください。

POTENTIOMETER

13279823 (trimmer)	UBJXB-20KB x 2		joy stick
13299202	EVN-D4AA00B23	2kB	LCD
13299197 (slide)	EVN-D4AA00B15	100kB	D/A
13359355	EWA-NAOX10B14		VOLUME, AFTERTOUCH

THERMISTOR

15229908	SDT-1000	

INDUCTOR

12449273	BL03RN2-R62	dyna scan board
12449294	BL03RN2-R62T2	main board jack board
12449291	BL02RN1-R62	power board
12449301	SN3-300 20μH	main board dyna scan board

FILTER

22445293	TFB-3 fc=14.5KHz	LC filter
12449299	ESD-R-19D	data line filter
12449298	ESD-R-25D	data line filter
13529149	ELXTV103EA	jack board
13529148	DSR1100-56E222MVA2EA	power board
12449229	FKOB-160MH15	power board
13529150	DSS310-55BB101M	power board

OPTOISLATOR

15229718	6H137		jack board

CRYSTAL

12389774	HC49/U-70	32.768MHz	synthe chip
12389765	TQC-226A-6R	12MHz	CPU

RESISTOR ARRAY

13919185 (chip)	RKM6L 103F 10k x 6		
15399910	MNRDM8-JX682E	6.8k x 8	main board
15399908	MNRDM2-JX153E	15k x 2	main board
15399907	MNRDM4-JX153E	15k x 4	main board
15399906	MNRDM8-JX153E	15k x 8	main board

CAPACITOR ARRAY

13529141	CN3Q9E220K	22P x 8	

CAPACITOR

13529132	RPE132-901F104Z25	0.1μF 25V	ceramic
13529143	DD306-F104Z25	0.1μF 25V	ceramic
13519452	DD306-959F104Z25	0.1μF 25V	ceramic
13659216M0	ECE SIEV682K	6800μ/25V	
13639195J0	SME35VB2200	2200μ/35V	
13529104	DE7150F472MVA1		line bypass

IC

(main board)			
15179261	μPD78312-07		CPU
15179266	μPD78312-022		CPU
	**See CHANGE INFORMATION and specify revision number, when ordering, to prevent incompatible problem.*		
	発注の際は，変更案内を参照の上，適切なバージョンを明記して下さい（互換性の確認）。		
15229851	MB87136		sythe chip
15179835	TC532000-7469Z		PCM ROM (A)
15179836	TC532000-7470Z		PCM ROM (B)
15179798	MBM27C512		PROM
	**See CHANGE INFORMATION and specify revision number, when ordering, to prevent compatible problem.*		
	発注の際は，変更案内を参照の上，適切なバージョンを明記して下さい（互換性の確認）。		
15179369	HM6264ASP		SRAM
15179374H0	HM62256LP		SRAM
15179380	μPD41416		DRAM
15219162	PCM54		D/A Converter
15229842	MB87137		chorus chip
15229849	HG61H25B18F		gate array
15229848	μPD65005G-062		gate array
15229866	MB87126-006		reverb chip
15259701T0	TC74HC00F-T2		quad 2-input NAND gate
15259709T0	TC74HC10F-T2		triple 3-input NAND gate
15259740T0	TC74HC139F-T2		dual 2-to-4 line decoder
15259757T0	TC74HC174F-T2		hex D-type flip flop with clear
15259102	μPD4066BG		quad bilateral switch
15289106	M5238FP		low noise OP amp (dual in line)
15289105	μPC4570G		low noise OP amp (dual in line)
15289110	μPC4062G		J-FET OP amp (dual inline)
(dyna scan board)			
15179343S0	LC3517AS-12		SRAM
(power board)			
15199156	M5F78M12		voltage ragulator
15199157	M5F79M12		voltage ragulator
15199155	L78MR05R		voltage ragulator

DIODE

15019125	1SS133	panel board
150196120X	0.5-5.1X	zener
15019281	1SR35-100A T-93	100V 1A
150192455N	S1VB10	100V 1A rectifier
15019272	2B4B41	100V 2A bridge rectifier
(chip)		
15339103	MA153	main board
15339105	DAN202K	main board
(LED)		
15029222	SLR-55VC3F red	bender board panel board

HOLDER

12199570	BBH-1 Battery Retainer	main board
22195925	Card Slot	card board
22195954	Card	
22195953	Joy stick	
22195952	LCD	
22195889	*MIDI	
22195951	*Jack	
22195955	Side L	
22195956	Side R	
22195950	Power transformer	power supply board

Attaching parts to Jack board.
ジャック・ボード付属品

CONNECTOR

(straight type)			
13439260	5267-03A	3P	wafer assy
13439263	5267-06A	6P	wafer assy
13439264	5267-07A	7P	water assy
13439523	5138-08APB	8P	black type
13439522	3024-08CHPB	8P	white type
13439326	5219-02A	2P	power board
13439306	5566-06A	6P	power board
(straight type)			
13439332	IL-S-5P-S2T2-EF	5P	connector pin header
13439335	IL-S-6P-S2T2-EF	6P	connector pin header
13439296	IL-S-7P-S2T2-EF	7P	connector pin header
13439297	IL-S-8P-S2T2-EF	8P	connector pin header
13439345	IL-S-9P-S2T2-EF	9P	connector pin header
13439337	IL-S-13P-S2T2-EF	13P	connector pin header
13439339	IL-S-15P-S2T2-EF	15P	connector pin header
(right angle type)			
13439349	IL-S-4P-S2L2-EF	4P	connector pin header
13439351	IL-S-6P-S2L2-EF	6P	connector pin header
13439354	IL-S-9P-S2L2-EF	9P	connector pin header
13439359	IL-S-14P-S2L2-EF	14P	connector pin header
13439364	IL-FPC-5S-4-SILI		aftertouch flat cable
13429191			memory card

MISCELLANEOUS

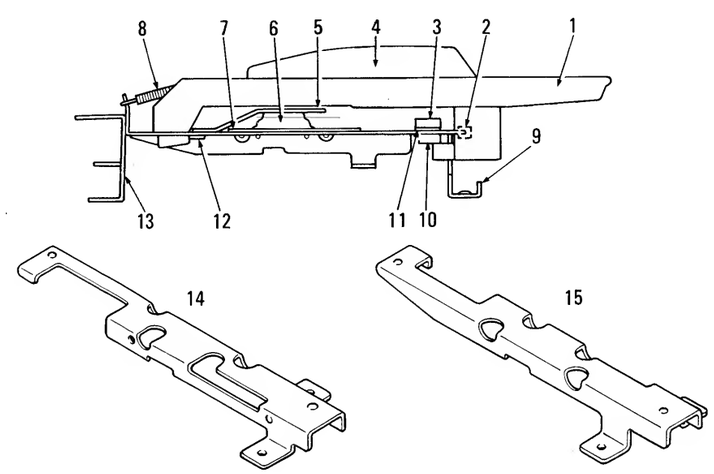
23455314	Grounding Reaf	
22345219	Insulating Shield	jack board
22255250	Shield Paper	side pabel R
22255252	Shield Paper	main board

BATTERY

12569249	CR2032 Leadless	lithium

MEMORY CARD

12379401	PN-D50-00 ROM	accessory



KEYBOARD
76180200 SK-361-PW 61 keys, with Velocity and Aftertouch

No.	PART No.	PART NAME	No.	PART No.	PART NAME
1	22575213	Natural key A	7	7616125000	Key Switch Assy (29P)
	22575214	Natural key D		7618024000	Key Switch Assy (32P)
	22575215	Natural key G	8	22175176	Key Spring (natural)
	22575216	Natural key C, F		22175177	Key Spring (sharp)
	22575217	Natural key E, B	9	22815575	Chassis
	22585218	Natural key C', F'	10	22265403	Stop Felt
2	22155716	Guide Bushing	11	23165676	Aftertouch Assy
3	22265451	Step Felt	12	22135415	Key Stopper A (long)
4	22575212	Sharp Key		22135416	Key Stopper B (middle)
5	22245144	Switch Cover (29P)		22135417	Key Stopper C (short)
	22245145	Switch Cover (32P)	13	22125572	Angle
6	22185218	Key Switch (12P)	14	22125569	Angle D
	22185219	Key Switch (13P)	15	22125570	Angle E

CHANGE INFORMATION

SOFTWARE REVISION

(CPU, PROM and Owner's Manual)
Since the introduction of the D-50 PROM (IC22, Main board) and CPU (IC25, Main board) have been revised for implementing improvements and new features. The table below lists the revisions and key improvements so far done as of this note.
ROM revision 2.00 involes a CPU change and both ICs are software incompatible with their predecessor(s), respectively.
ROM revision 2.10 gives the D-50 new features which cause a release of new edition of Owner's Manual to describe the new functions.
The Roland makes new features available to early users (Ver. 1.07 or below) by providing ROM Ver. 1.10 that contains the new features as well as the updates.

PROM Ver.	CPU	What is improved
1.04	μ PD-78312G-017 15179261	
1.05		Increased output level.
1.06		Changing PATCHES sometimes also changes OUTPUT MODES ; Ver. 1.06 cures this problem. There is no audible difference between CHORUS types 5 and 6 ; Ver. 1.06 contains modified 5.
1.07		Reduced noise in chorus sounds. The effect of KEYFOLLOW on TVF ENV DEPTH is opposite to what designed. Ver. 1.07 cures this problem.
1.10		For replacement use only. When a customer having Ver. 1.0X wants updated feature as described for Ver. 2.10 in this table, use. 1.10.
2.00	μ PD-78312G-022 15179266	Increase arithmetic operation speed by employing new CPU.
2.10		Change the way of setting separate channel. Add the following features. ・ Program Change Number can be transmitted. ・ Patch Dump can be made through exclusive message. ・ Portamento and Hold effects can be given independently on each tone in DUAL KEY MODE.

Replacement Considerations

Ver. 1.07 and below
Use Ver. 1.10 when adding new features found on Ver. 2.10. In this case the user should be informed of the new features by the supporting documents (A supplementary Owner's manual and edit map).
μPD-78312G-017 cannot be replaced by -022 type.
ROM Ver. 1.10 or below cannot be replaced by Ver. 2.00 or up.

Ver. 2.00
Use Ver. 2.10 when adding new features. In this case the user should be informed of the new features by the supporting documents (A supplementary Owner's manual and edit map).

変更案内

ソフトウェアーのバージョン・アップ

D-50 では，発売後下記に示すプログラム変更があり，CPU(IC25) および PROM(IC22) のバージョン・アップが行なわれています。
PROM Ver.2.00 以降の変更は，CPU の変更を伴なっており，PROM や CPU は以前のものと互換性がありません。交換の際は組み合せに注意するとともに，発注の際はバージョン・ナンバーを必ず明記して下さい。

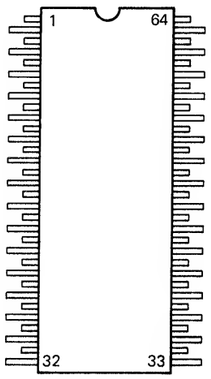
PROM Ver.	CPU	改 良 点
1.04	μ PD-78312G-017 15179261	
1.05		出力レベルを上げる
1.06		パッチを切り換えた時，アウトプット・モードの設定が変ることがある，これを修正 コーラス・タイプの 5 と 6 が同一内容，5 を変更
1.07		コーラスのノイズ対策 TVF ENV デプス・キーフォローの変化逆，これを修正
1.10		スペックのバージョン・アップ対策用（補修専用） Ver.2.10 と同一スペック
2.00	μ PD-78312G-022 15179266	演算処理の高速化
2.10		スペックのバージョン・アップ 1)セパレート・チャンネルの設定の仕方変更。 2)プログラム・チェンジ・ナンバーの送信機能追加。 3)エクスクルーシブ・メッセージによるパッチ・ダンプの機能追加。 4)キー・モードがデュアルの時，ポルタメントとホールド効果が各トーンごとに独立して設定可能になる。

スペックのバージョン・アップを行なう場合

1） Ver.1.07までのものは，Ver.1.10 に交換して下さい。
Ver.2.00 のものは，Ver.2.10 に交換して下さい。
2）新しいスペックに関する補足オーナーズ・マニュアルおよびエディット・マップを付けて下さい。

IC DATA

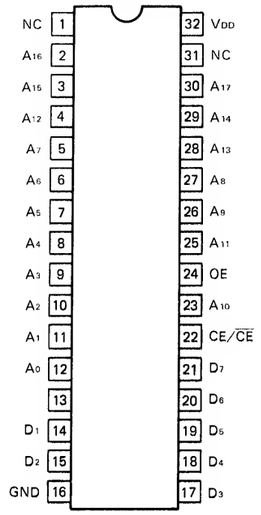
CPU μPD78312



TOP VIEW

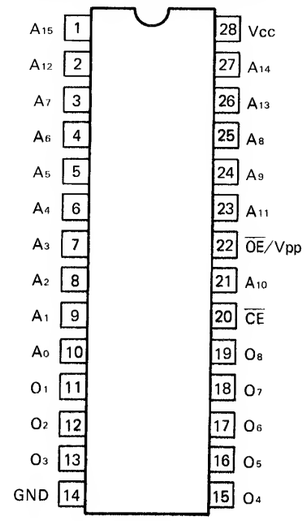
No	NAME	I/O	No	NAME	I/O	No	NAME	I/O	No	NAME	I/O
1	P0.0	O	17	NMI	I	33	AN0	I	49	A14	O
2	P0.1	O	18	INT0	I	34	AN1	I	50	A15	O
3	P0.2	O	19	INT1	I	35	AN2	I	51	$\overline{EA}$	I
4	P0.3	O	20	INT2	I	36	AN3	I	52	$\overline{RESET}$	I
5	P0.4	O	21	T X D	O	37	AVREF	O	53	$\overline{RD}$	O
6	P0.5	O	22	R X D	I	38	AVss	-	54	$\overline{WR}$	O
7	P0.6	O	23	$\overline{SCK}$	O (NC)	39	P3.4	I/O(NC)	55	ALE	O
8	P0.7	O	24	$\overline{CTS}$	I/O	40	P3.5	I/O(NC)	56	AD0	I/O
9	P1.0	I/O	25	$\overline{RFSH}$	O (NC)	41	P3.6	I/O	57	AD1	I/O
10	P1.1	I/O	26	P3.0	I	42	P3.7	I/O	58	AD2	I/O
11	P1.2	I/O	27	P3.1	I	43	A8	O	59	AD3	I/O
12	P1.3	I/O	28	P3.2	I	44	A9	O	60	AD4	I/O
13	P1.4	I/O	29	P3.3	I	45	A10	O	61	AD5	I/O
14	P1.5	I/O	30	X1	I	46	A11	O	62	AD6	I/O
15	P1.6	I/O	31	X2	I	47	A12	O	63	AD7	I/O
16	P1.7	I/O(NC)	32	Vss	-	48	A13	O	64	VDD	-

PCM ROM A/B TC532000



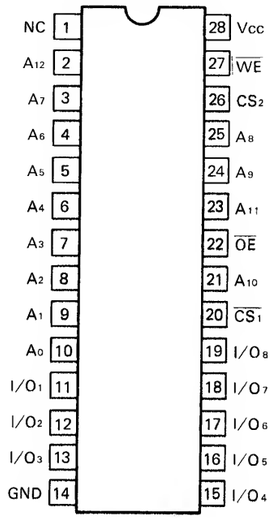
TOP VIEW

EP ROM MBM27C512



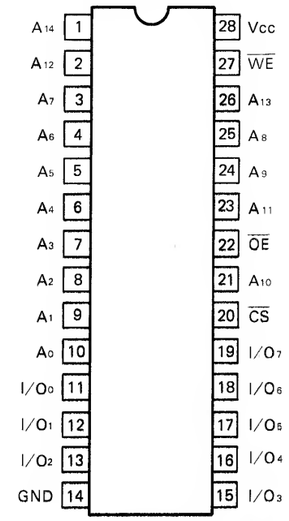
TOP VIEW

S RAM HM6264ASP



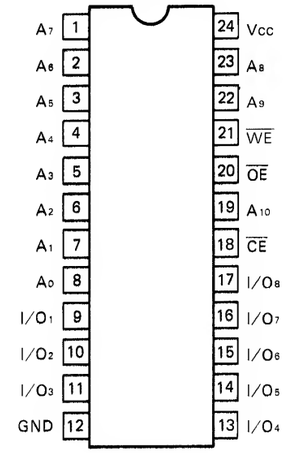
TOP VIEW

S RAM HM62256LP



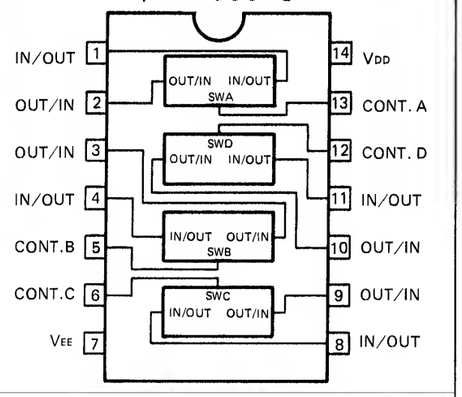
TOP VIEW

S RAM LC3517AS



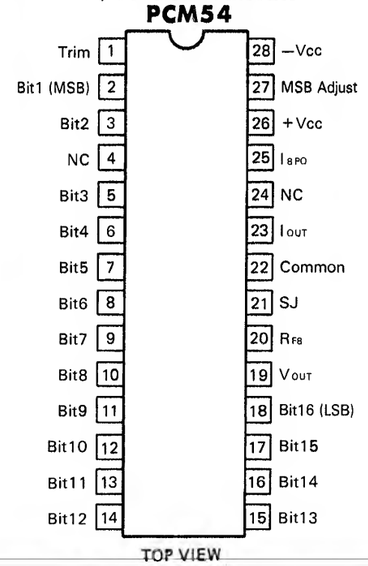
TOP VIEW

μPD4066BG



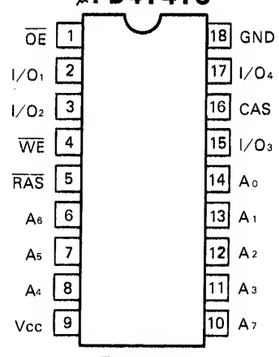
TOP VIEW

D/A CONVERTER PCM54



TOP VIEW

D RAM μPD41416

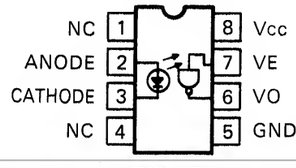


TOP VIEW

μPC4062G μPC4570G M5238FP

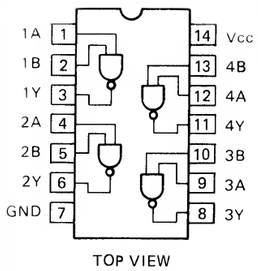
TOP VIEW

6N137



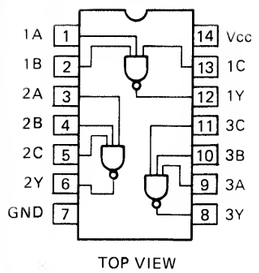
TOP VIEW

74HC00



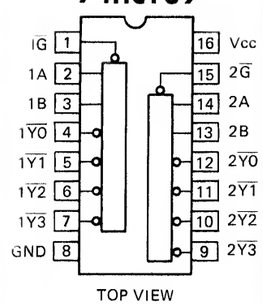
TOP VIEW

74HC10



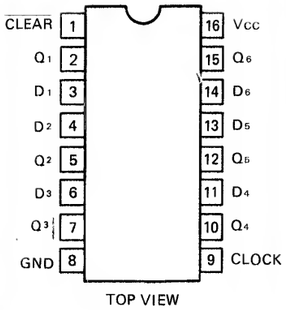
TOP VIEW

74HC139



TOP VIEW

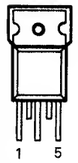
74HC174



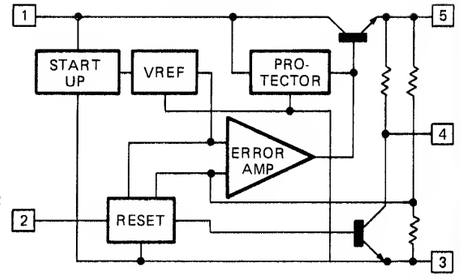
TOP VIEW

L78MR05R

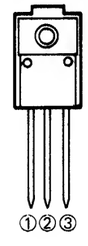
FRONT VIEW



1 INPUT
2 DELAY CAPACITOR
3 GND
4 RESET OUTPUT
5 OUTPUT



M5F78M12 (M5F79M12)



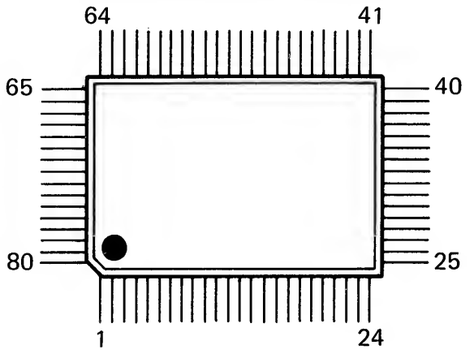
1. INPUT
2. GND (INPUT)
3. OUTPUT

FRONT VIEW

①②③

IC DATA

REVERB CUSTOM IC
MB87126-006

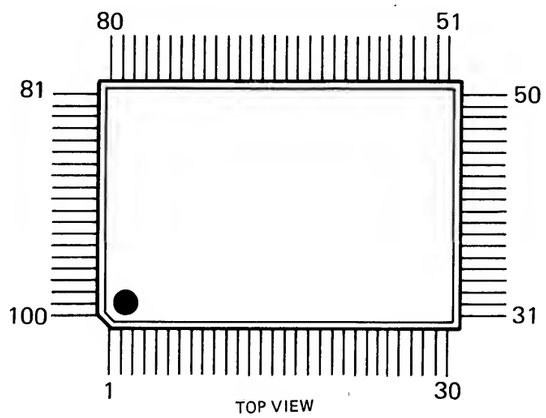


TOP VIEW

PIN.NO.	PIN NAME	I/O	DESCRIPTION
1、2、66～72、74～80	DC0-15	O	Data output for chorus chip and DAC D/A へのデータ，コーラス・データ出力端子
3	STRT	I	Pulled low GND にプルダウン
4	DIN	I	Pulled low GND にプルダウン
5	CLEA	I	Pulled low GND にプルダウン
6～10	RD0-4	O	Control output for enable and for S/H and Lower for bit D/A Conversion コントロール出力端子 イネーブル，S/H，D/A（下 4 bit）
11	RSET	I	Pulled low GND にプルダウン
12, 15, 36 52, 65	Vss	–	GND
13	SLRO	I	Pulled low GND にプルダウン
14	MSCK	I	Master clock input マスター・クロック入力端子
16	SLCK	O	Not used 未使用
17	TEST	I	Pulled low GND にプルダウン
18	TMB	O	Time base signal output タイム・ベース信号出力端子
19、33、73	V_{DD}	–	＋5 V

PIN.NO.	PIN NAME	I/O	DESCRIPTION
20	$\overline{LOAD}$	O	Sync signal output シンク信号出力端子
21	SYNC	I	Sync signal input シンク信号入力端子
22	INCK	I	Data latch clock input for initialization イニシャライス時のデータ・ラッチ・クロック入力端子
23	ERCL	I	Busy veset output Busy　解除用端子
24	BUSY	O	Serial data transfer errov output (Parity check) シリアル・データ転送エラー出力 （パリティー・チェック）
25	SXD	I	Serial data input シリアル・データ入力端子
26	SCK	I	Serial data read-in clock input シリアル・データ取込みクロック入力端子
27 - 32, 34、35、	DAO-7	O	Connect to RAM address bus RAM アドレス・バス
37	$\overline{RAS}$	O	Row address strobe output ロー・アドレス・ストローブ
38	$\overline{WE}$	O	DRAM write pulse output DRAM ライト・パルス出力端子
39	$\overline{CAS}$	O	Column address strobe output カラム・アドレス・ストローブ
40 - 51, 53 - 64、	DRO-23	I/O	Connect to RAM data bus Synth and Chorus data input RAMデータ・バス，シンセ，コーラスデータ入力端子

CHORUS CUSTOM IC
MB87137



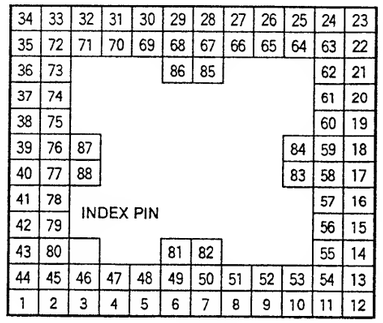
TOP VIEW

PIN.NO.	PIN NAME	I/O	DESCRIPTION
1	RES	I	Reset input ； pulled up to V_{DD} リセット入力端子　V_{DD}にプルアップ
2	E	I	Chip enable input ； pulled up to V_{DD} チップ・イネーブル入力端子　V_{DD}にプルアップ
3，28，53 78	V_{DD}	–	＋5V
4	CS	I	Chip select input ； pulled up to V_{DD} チップ・セレクト入力端子　V_{DD}にプルアップ
5	$\overline{RW}$	I	Write pulse input ライト・パルス入力端子
6	$\overline{RD}$	I	Read pulse input リード・パルス入力端子
7	$\overline{CS}$	I	Chip select input チップ・セレクト (LOW) 入力端子
8 - 10	A0-2	I	Connect to CPU address bus CPU とのアドレス・バス
11 - 14、16 - 19、	D0-7	I/O	Connect to CPU data bus CPU とのデータ・バス
15，40，65 87、90	Vss	–	GND
20	$\overline{DOE}$	I	Data out enable input データ・アウトプット・イネーブル入力端子
21	INCK	I	Input data latch clock input データ入力用ラッチクロック入力端子
22	SIN	I	Sync input ； pulled up to V_{DD} シンク信号入力端子　V_{DD}にプルアップ
23	SOUT	O	Sync output シンク信号出力端子
24	LRS	I	L/R select input L/R　セレクト
25 - 27、29 - 39、41 - 42、	IO-15	I	Data input データ入力端子
43 - 52、54 - 59	O0-15	O	Data input データ入力端子
60、62 - 64、66 - 70、72 - 74、76 - 79	**RAO-13**	O	Connect to SRAM address bus RA13 not used SRAM アドレス・バス　RA13 未使用

PIN.NO.	PIN NAME	I/O	DESCRIPTION
61	$\overline{WE}$	O	SRAM write pulse output SRAM 用　ライト・パルス出力端子
71	$\overline{OE}$	O	SRAM out enable output SRAM 用　アウトプット・イネーブル出力端子
75	$\overline{CE}$	O	SRAM chip enable output SRAM 用　チップ・イネーブル出力端子
77、80 - 86	PD7-O	I/O	Connect to SRAM data bus SRAM データ・バス
88	X1	I	Master clock input マスター・クロック入力端子
89	X2	O	Not used 未使用
91	ROMT	I	Pulled IOW テスト端子　GND にプルダウン
92	RAMT	I	
93	CTRT	I	
94	THRU	I	
95	ECTL	I	External control select input ； pulled up to V_{DD} エクスターナル・コントロール・セレクト入力端子 V_{DD}にプルアップ
96	ADDA	I	Pulled low テスト端子　GND にプルダウン
97	OFST	I	OFFset binary select input ； pulled up to V_{DD} オフセット・バイナリー・セレクト V_{DD}にプルアップ
98	PSFT	I	Pulled low テスト端子　GND にプルダウン
99	LHLD	O	Signal output for S/H ； not used S/H 用信号出力端子　未使用
100	RHLD	O	Signal output for S/H ； not used S/H 用信号出力端子　未使用

IC DATA

SYNTHE CUSTOM IC
MB87136

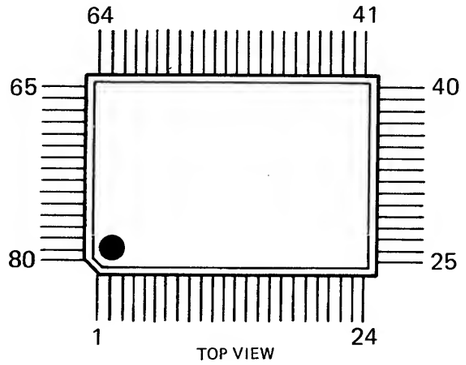


TOP VIEW

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	$\overline{CS}$	I	Chip select チップ・セレクト入力端子
2 - 6, 46 - 49.	A0-8	I	Connect to CPU address bus CPU とのアドレス・バス
7 - 10, 50 - 53.	D0-7	I/O	Connect to CPU data bus CPU とのデータ・バス
11 - 14, 54 - 57.	PD0-7	I	Connect to ROM data bus ROM とのデータ・バス
15 - 26, 58 - 65.	RA0-19	O	Connect to ROM address bus ROM とのアドレス・バス
27 - 35, 66 - 72.	O0-15	O	Data output テータ・アウトプット・バス
36 - 37, 73 - 74.	SH0-3	O	Not used 未使用
38	——	—	Not used 未使用
39	X1	I/O	Xtal input (32.768 MHz) 水晶振動子 (32.768 MHz) 接続端子
40	32M	O	The same frequency as that of master clock マスター・クロックと同じ周波数を出力
41	——	—	Not used 未使用
42	$\overline{SYI}$	I	Sync signal input シンク信号入力端子
43	$\overline{WR}$	I	Write pulse input ライト・パルス入力端子

PIN NO.	PIN NAME	I/O	DESCRIPTION
44	$\overline{INT}$	O	Interrupt output インタラプト　出力端子
45	$\overline{OE}$	I	Output enable input アウトプット・イネーブル入力端子
75	——	—	Not used 未使用
76	X2	I/O	Xtal input 水晶振動子 (32.768 MHz) 接続端子
77	16M	O	Output frequency is one half of master clock マスター・クロックを 1 回分周した周波数を出力
78	CKIN	I	lutput frequency is a combination of the master clock and one half of master clock マスター・クロックと 1 回分周した周波数を出力 Not used
79	——	—	Not used 未使用
80	$\overline{RD}$	I	Read pulse input リート・パルス入力端子
81, 84, 85, 88,	Vss	—	GND
82, 83, 86, 87,	V_{DD}	—	+5 V

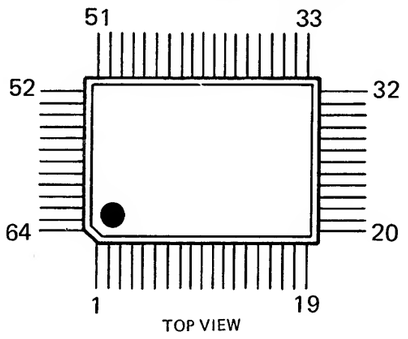
GATE ARRAY
HG61H25B18F



TOP VIEW

PIN NO.	NAME	I/O	PIN NO.	NAME	I/O	PIN NO.	NAME	I/O	PIN NO.	NAME	I/O
1	SYNT2	O (NC)	21	ALE	I	41	EC	O	61	R2	I
2	IRAM	O (NC)	22	$\overline{WR}$	I	42	O0	O	62	R3	I
3	RAM	O	23	$\overline{RD}$	I	43	O1	O	63	R4	I
4	A7	O	24	$\overline{RESET}$	I	44	O2	O	64	R5	I
5	A6	O	25	A15	I	45	O3	O	65	R6	I
6	A5	O	26	A14	I	46	O4	O	66	R7	I
7	A4	O	27	A13	I	47	O5	O	67	CORUS	O
8	A3	O	28	A12	I	48	O6	O	68	SCK	O
9	A2	O	29	A11	I	49	O7	O	69	SXD	O
10	A1	O	30	A10	I	50	S0	O	70	BUSY	I
11	A0	O	31	A9	I	51	S1	O	71	ERCL	O
12	Vss	-	32	A8	I	52	Vss	-	72	LOAD	I
13	AD7	I/O	33	V_{DD}	-	53	S2	O	73	V_{DD}	-
14	AD6	I/O	34	ARS	I (HIGH)	54	S3	O	74	TMB	I
15	AD5	I/O	35	INT1	O (NC)	55	S4	O	75	SINT1	I (LOW)
16	AD4	I/O	36	INT2	O	56	S5	O	76	SINT2	I (LOW)
17	AD3	I/O	37	DSCAN	O	57	S6	O	77	TEST1	I (LOW)
18	AD2	I/O	38	$\overline{ERAM}$	O	58	S7	O	78	CLK	I
19	AD1	I/O	39	ERAM	O (NC)	59	R0	I	79	TEST2	I (LOW)
20	AD0	I/O	40	RS	O	60	R1	I	80	SYNT1	O

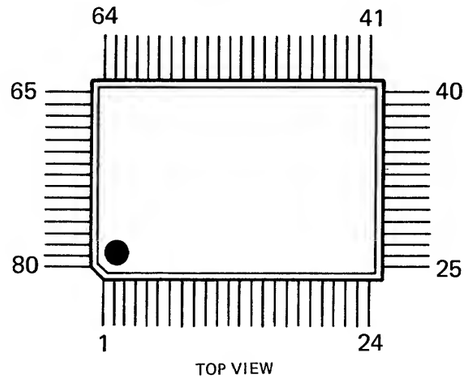
GATE ARRAY
μPD65005G-062



TOP VIEW

PIN NO.	NAME	I/O	PIN NO.	NAME	I/O	PIN NO.	NAME	I/O	PIN NO.	NAME	I/O
1	NC	-	17	NC	-	33	NC	-	49	NC	-
2	NC	-	18	NC	-	34	NC	-	50	CD0	I/O
3	AD7	I/O	19	A13	I	35	CA5	O	51	CD1	I/O
4	AD6	I/O	20	A12	I	36	CA6	O	52	CD2	I/O
5	AD5	I/O	21	A11	I	37	CA7	O	53	CD3	I/O
6	AD4	I/O	22	A10	I	38	CA8	O	54	CD4	I/O
7	AD3	I/O	23	A9	I	39	CA9	O	55	CD5	I/O
8	AD2	I/O	24	A8	I	40	CA10	O	56	CD6	I/O
9	AD1	I/O	25	SEL	I (LOW)	41	CA11	O	57	CD7	I/O
10	AD0	I/O	26	Vss	-	42	CA12	O	58	Vss	-
11	Vss	-	27	V_{DD}	-	43	CA13	O	59	V_{DD}	-
12	V_{DD}	-	28	CA0	O	44	CA14	O	60	BATT	I (LOW)
13	ALE	I	29	CA1	O	45	MR	O	61	SENS	I (NC)
14	$\overline{WR}$	I	30	CA2	O	46	CWR	O	62	RCS	I
15	$\overline{RD}$	I	31	CA3	O	47	CCS	O	63	$\overline{CS}$	I
16	A14	I	32	CA4	O	48	CRD	O	64	NC	-

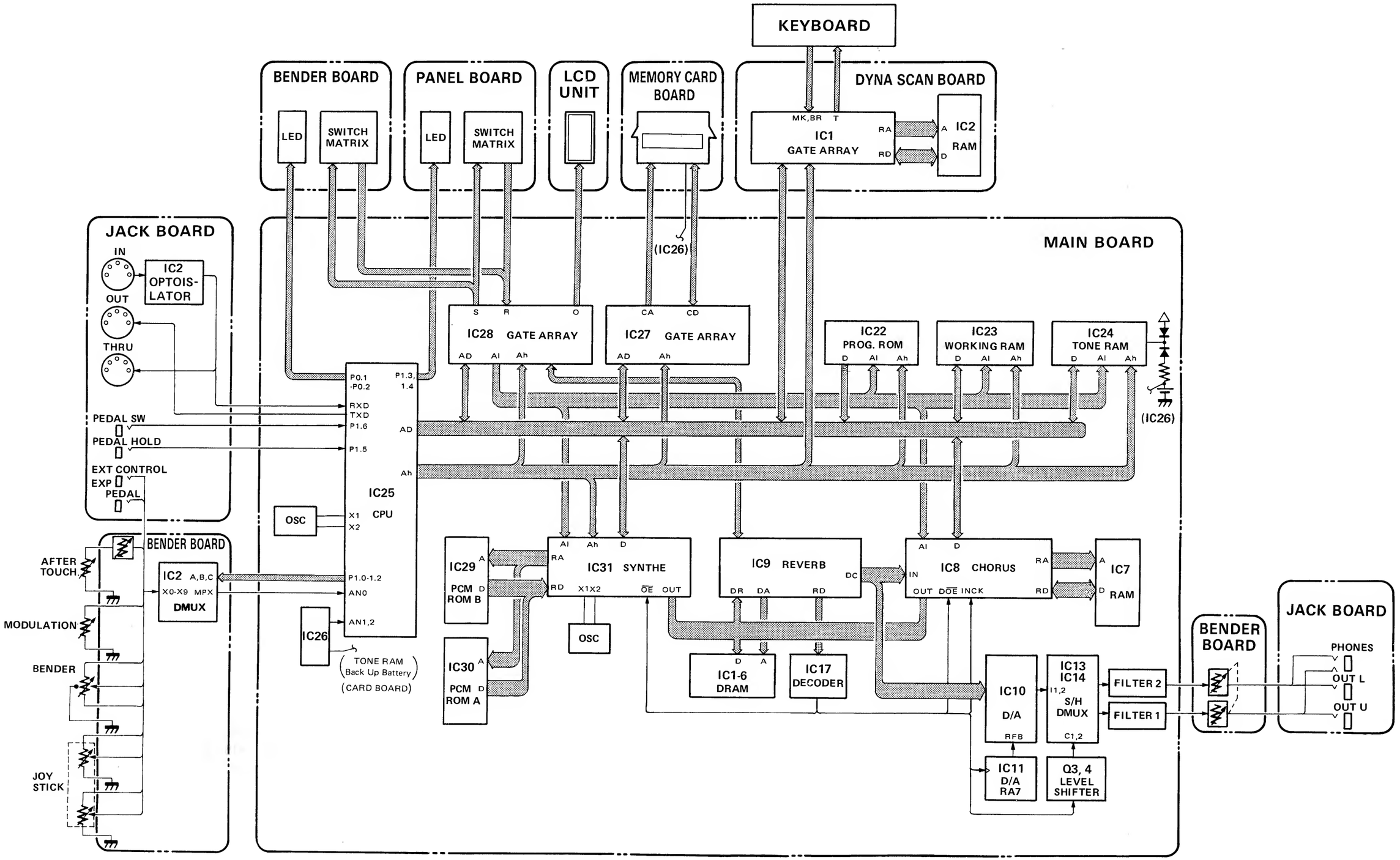
GATE ARRAY
MB63H149



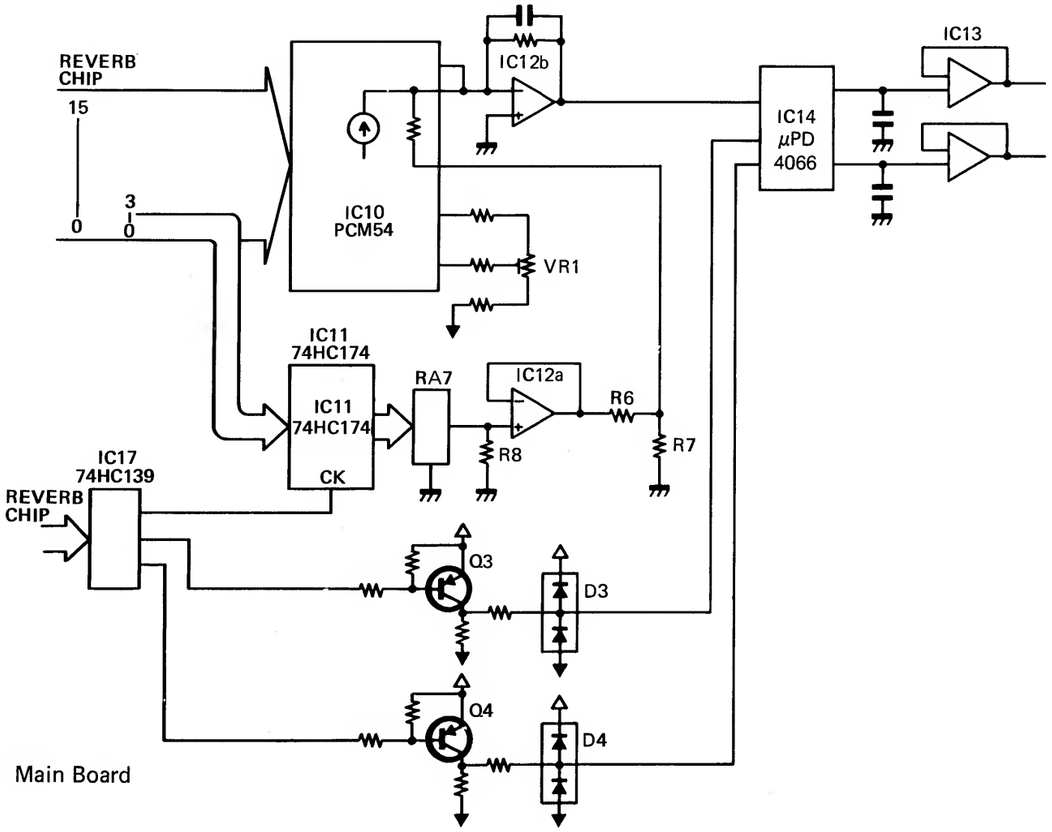
TOP VIEW

PIN NO.	NAME	I/O	PIN NO.	NAME	I/O	PIN NO.	NAME	I/O	PIN NO.	NAME	I/O
1	T7	O	21	BR9	I	41	AD7	I/O	61	RA1	O
2	BR0	I	22	MK9	I	42	CA8	I	62	RA10	O
3	MK0	I	23	BR10	I	43	CA9	I	63	RA2	O
4	BR1	I	24	MK10	I	44	CA10	I (LOW)	64	$\overline{ROE}$	I/O
5	MK1	I	25	RES	I	45	CS	I	65	RA3	O
6	BR2	I	26	$\overline{EXCK}$	I/O	46	XT1	I	66	$\overline{RWE}$	O
7	MK2	I	27	E	I (HIGH)	47	XT2	O (NC)	67	RA4	O
8	BR3	I	28	INT	O	48	ASEL	O (NC)	68	RA9	O
9	MK3	I	29	AS	I	49	MOD1	I (HIGH)	69	RA5	O
10	BR4	I	30	$\overline{CRES}$	O (NC)	50	MOD2	I (LOW)	70	RA8	O
11	MK4	I	31	$\overline{CRNW}$	I	51	RD3	I/O	71	RA6	O
12	Vss	-	32	SRCK	O (NC)	52	Vss	-	72	RA7	O
13	BR5	I	33	V_{DD}	-	53	RD4	I/O	73	V_{DD}	-
14	MK5	I	34	AD0	I/O	54	RD2	I/O	74	T0	O
15	BR6	I	35	AD1	I/O	55	RD5	I/O	75	T1	O
16	MK6	I	36	AD2	I/O	56	RD1	I/O	76	T2	O
17	BR7	I	37	AD3	I/O	57	RD6	I/O	77	T3	O
18	MK7	I	38	AD4	I/O	58	RD0	I/O	78	T4	O
19	BR8	I	39	AD5	I/O	59	RD7	I/O	79	T5	O
20	MK8	I	40	AD6	I/O	60	RA0	O	80	T6	O

BLOCK DIAGRAM



Digital to Analog Conversion (20bits)



Main Board

IC10	Upper 16 bits D/A Conversion 上位16 bit　D/A 変換
IC11	Lower 4 bits data latch 下位 4 bit　データ・ラッチ
RA7	Lower 4 bits D/A Conversion 下位 4 bit　D/A 変換
IC12a R6 R7 R8	Lower 4 bits Weighing 下位 4 bit の重み付け
VR1	MSB Weight adjuster MSB　重み調整
IC12b	I/V Conversion I/V 変換
IC14	Analog switch ; separates UPPER and LOWER UPPER と LOWER の信号に分ける アナログ・スイッチ
Q3 , D3 Q4 , D4	LEVEL SHIFTER
IC17	DECODER
IC13	S/H

Analog to Digital Conversion

The outputs from controls shown in the table are of analog value. They are first selected among them at bender board IC2 output by a code A, B and C. The analog output fed through IC3b to the CPU pin 33 is converted to the corresponding digital value by the CPU's internal DAC. The reference voltage (V_{REF}) for A/D conversion is being originated at IC4a of the bender board.

A／Dの変換

以下に示すコントロール機能の変化は，BENDER BOARD 上の IC2(4051) に読み込まれ，CPU から IC2 の A，B，C に与えられる 3bit のデータによって，どれを A/D 変換するかをセレクトされる。セレクトされたデータは，IC3b を通じて CPU に送られ，CPU 内で A/D 変換される。
A/D 変換の基準となるリファレンス電圧（V_{REF}+4.5 V）は，BENDER BOARD 上の IC4a で作られる。

Analog Control Voltages vs Digital Values

Control	Test Point BENDER BOARD(IC2)	Analog Reading and Digital Reading 電圧変化（テスト・モード時の数値）
MODULATION	Pin 5	Off 定常時　0V(00) ⟶ 4.8 V (127)　Pressed 押す
PITCH BENDER	Pin 1 or 13	LEFT　0V（＋00）　RIGHT 3.2 V_{P-P} (−127)　3.2 V_{P-P} (+127) Tilting toward right will produce a random rectangular. To the left a DC voltage. 右へ傾けたとき，矩形波状の電圧が出る。(ランダム周期)
JOYSTICK	Pin 14	V_{REF} (00)　0V (127)
	Pin 15	0V (127) V_{REF} (00)
AFTERTOUCH	Pin 4	Off 定常時　0V(00) ⟶ 4.7 V (127)　Pressed 押す AFTERTOUCH at the top AFTERTOUCH　ボリューム最大
EXT CONT	Pin 2	V_{REF}(127)　pedal disengaged ＝ 0V ペダルを接続しない状態＝ 0V 0V (00)
EXP PEDAL	Pin 12	V_{REF}(127)　pedal disengaged ＝ V_{REF} ペダルを接続しない状態＝ V_{REF} 0V (00)

INDENTIFYING ROM (IC22) VERSION NUMBER

Hold "0" button on Ten-keypad and INCREMENT then switch the power on. The display should show the current ROM version number as well as acknowledgment, then the instrument will enter into normal play mode.

バージョン・ナンバーの確認

TEN KEY と INCREMENT を押しながら，電源オン。しばらく下記の画面が表示された後，プレイ・モードの表示になる。

Version number

```
Ver.□□□□
Thanks to Eric & Adrian. ***************
```

ADJUSTMENT

1. LCD Contrast

1-1. Adjust VR2 (Main board) so that the LCD would give the best visibility to the keyboard player.

2. DAC

With monitor system connected to OUTPUT jack (U or L).

2-1. Hold "0" (Ten-keypad) and WRITE then switch the power on. The LCD should read:

```
****** L.A. Chip Test Mode V□□□******
Press [COMPARE] for D/A Adjustment mode.
```

2-2. Press COMPARE and the instrument will enter into adjustment mode. The unit will show a test titie while generating a low level test sound.

CAUTION
Don't touch UPPER (PARTIAL BALANCE) button. Pressing this button will generate a greater output (10V max).

調整

1．LCD コントラスト調整

通常の演奏状態の位置から文字がよく見える程度に VR2 で調整。

2．D/A 調整

アウトプット・ジャックにアンプを接続。

① TEN KEY の 0 と WRITE を押しながら電源オン。

② COMPARE を押すと，調整モードになる。
（下表の表示になるとともに，微小レベルの調整音が発音される。）

注意 !! UPPER (PARTIAL BALANCE) は押さないで下さい。
アウトプットから 10V が出力されます。

```
****** L.A. Chip Test Mode V□□□******
/*D/A Adjustment */
```

2-3. Raise VOLUME to top.

③ VOLUME ツマミを最大にする。

2-4. Adjust VR1 (Main board) for the minimum distortion.

④ VR1 で，歪が最小になるように調整。

2-5. Turn the power off.

⑤調整終了後は，電源をオフにする。

RECOVERING TONE RAM DATA

When the backup battery or RAM (IC24) has been replaced, take the following steps.

1. (Refer to D-50 Owner's Manual, Advance Course Page 66) Transfer PATCH and REVERB TYPE (17-32) data from the memory card (PN-D-50-00) to the internal memory.

2. Hold "0" (Ten-keypad) and DATA TRANSFER, then turn the power on. TUNE/FUNCTION and MIDI function data from ROM (IC22) will be stored into the RAM. The LCD will read "Complete" and then normal play mode message.

データの設定

バッテリーや TONE RAM (IC24) の交換などで，TONE RAM のデータが失われた場合に次の操作を行なう。

1．パッチやリバーブ・タイプ (17-32) のデータは，D-50 のオーナーズ・マニュアル（応用編 P 66）を参照の上，メモリー・カード (PN-D50-00) から本体メモリーへデータを転送する。

2．チューン／ファンクションや MIDI ファンクションのデータは，TEN KEY の 0 と DATA TRANSFER を押しながら，電源オンにしてイニシャライズする。
Complete としばらく表示された後，プレイ・モードの表示になる。

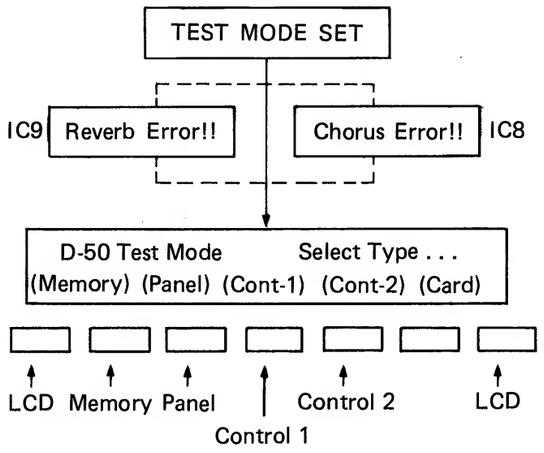
TEST MODE

CAUTIONS

Leave all sockets and card slot except for AC inlet Disengaged.

Hold "0" (Ten-keypad) and DECREMENT then turn the power on. The display will show Test Mode menu.

テストを行なう前は，ペダルの接続やメモリー・カードを挿入しない。
TEN KEY の 0 と DECREMENT を押しながら電源を入れると，テスト・メニュー画面が表示される。



Test Mode menu
テスト・モード・メニュー

If instead, an error message as shown by dotted line is displayed, there may be a problem with the respective IC. Pressing EXIT will force the test to go to the menu.

エラー・メッセージが表示された時は，該当する IC 周辺の不良。
そのまま次のステップへ進む時は，EXIT を押す。

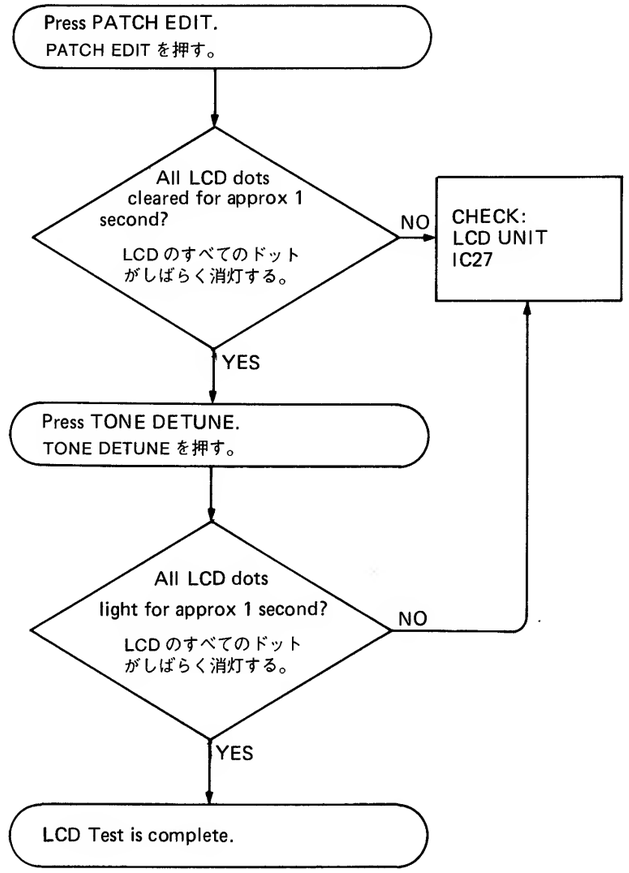
Without an error, the Test Mode menu should appear. The five buttons just below the LCD will serve as test routine selector. U-TONE EDIT (Card) has no effect in this test. Any test can be repeatedly performed.

テスト・メニュー画面には，各テスト項目が表示される。画面下のボタンでテスト項目を選択し，以下の操作でそれぞれのテストを行なう。(同一テストを繰り返して行なえる)

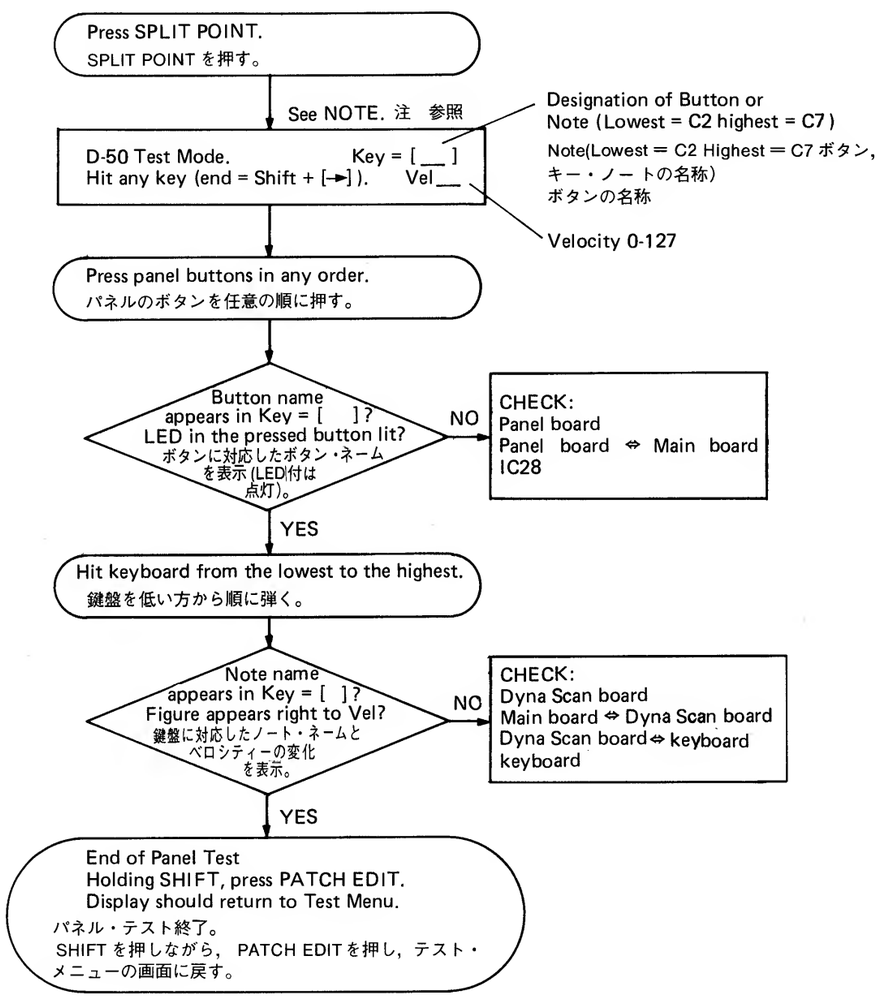
Buttons for returning to Test Mode menu.
- During Panel Test . . . . . .Press and hold SHIFT then PATCH EDIT.
- During Other Tests . . . . .Press EXIT.

テスト・メニュー画面への戻り方
Panel Test …… SHIFT を押しながら PATCH EDIT を押す。
その他…… EXIT を押す。

〔LCD TEST〕

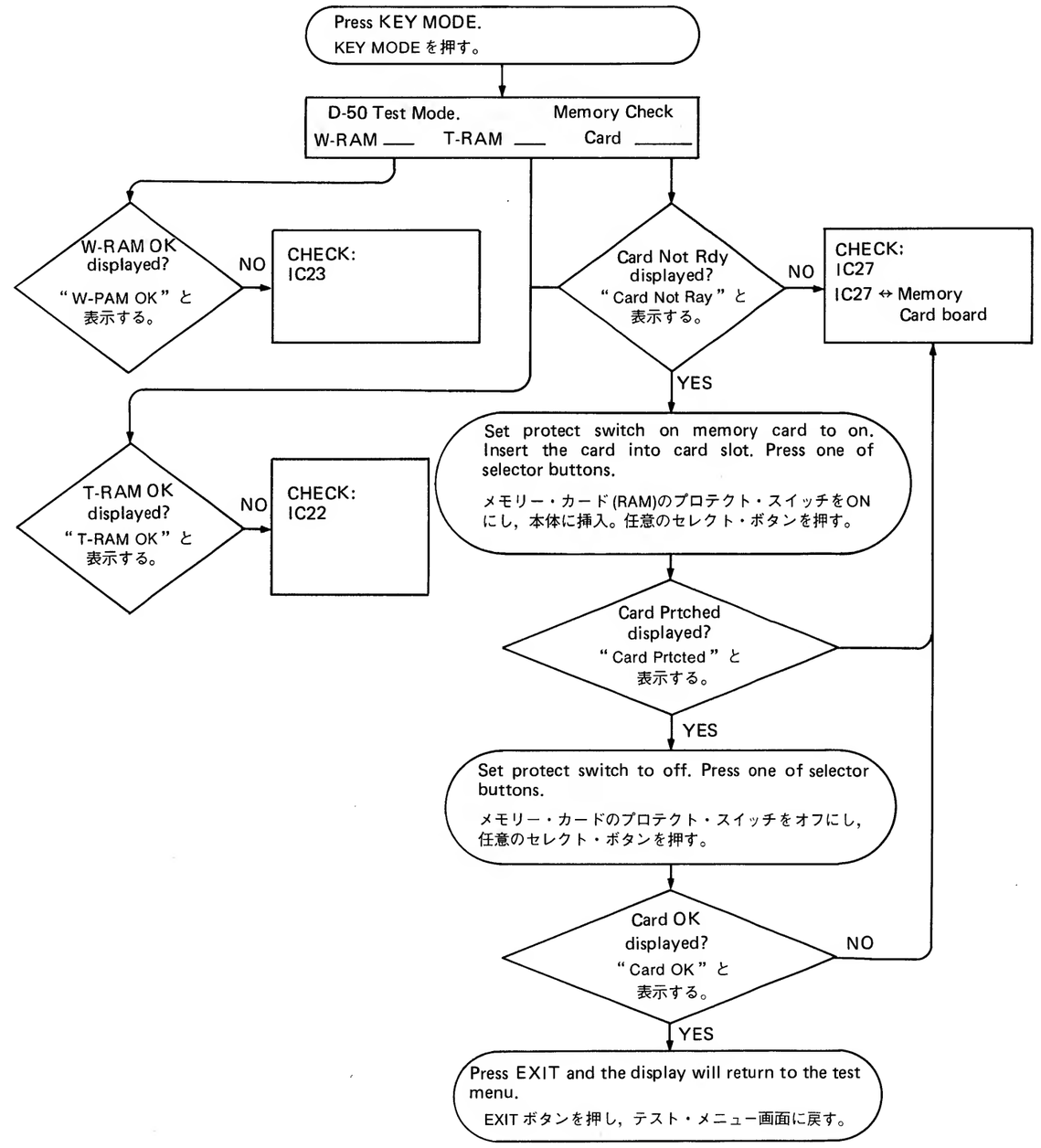


〔PANEL TEST〕

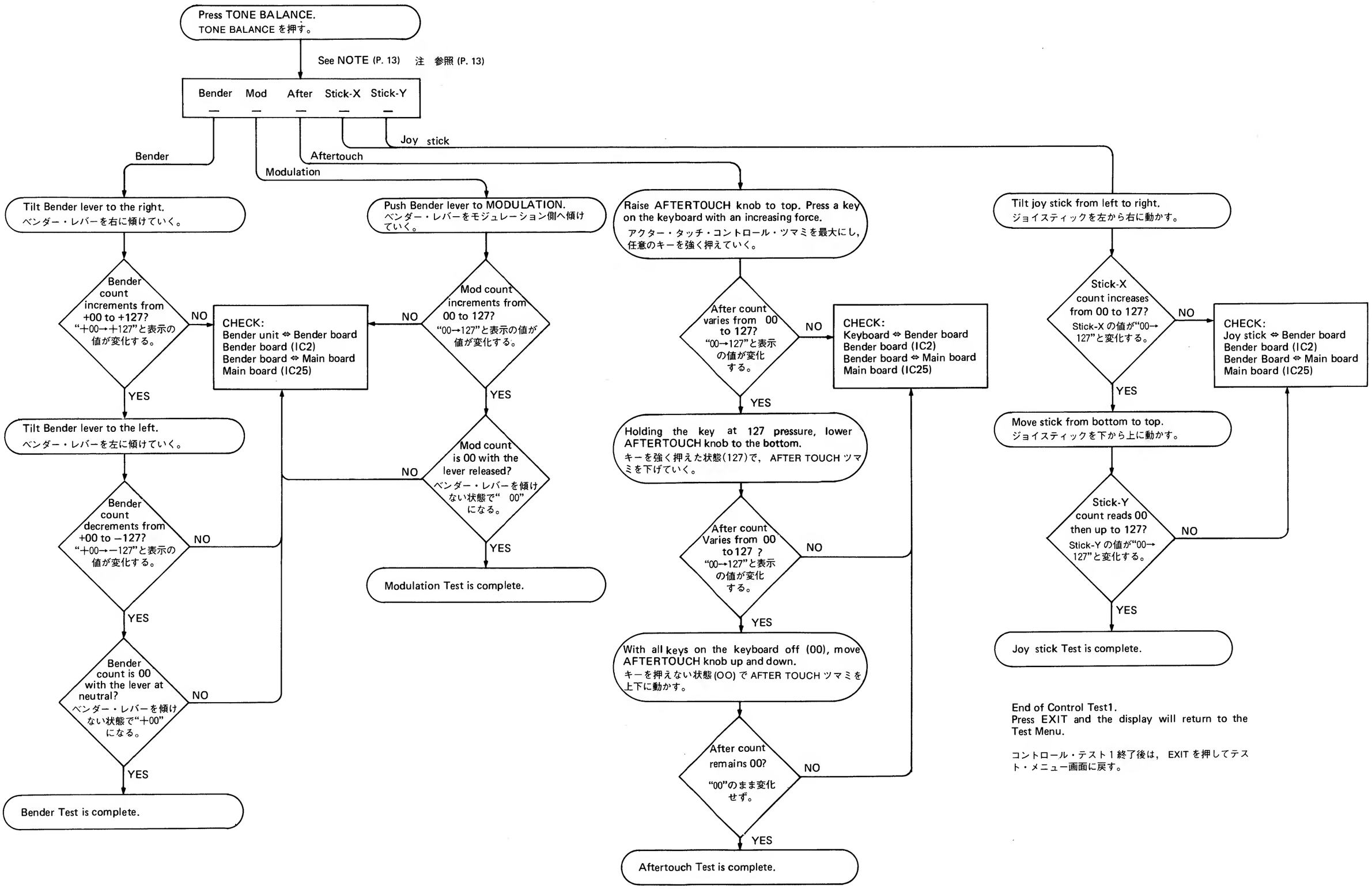


NOTE: Default values should be empty. Any figure indicates defective in corresponding circuit.

注 画面を呼び出した時は，数値は表示しない。何らかの数値が表示された時は，該当する箇所をチェック。



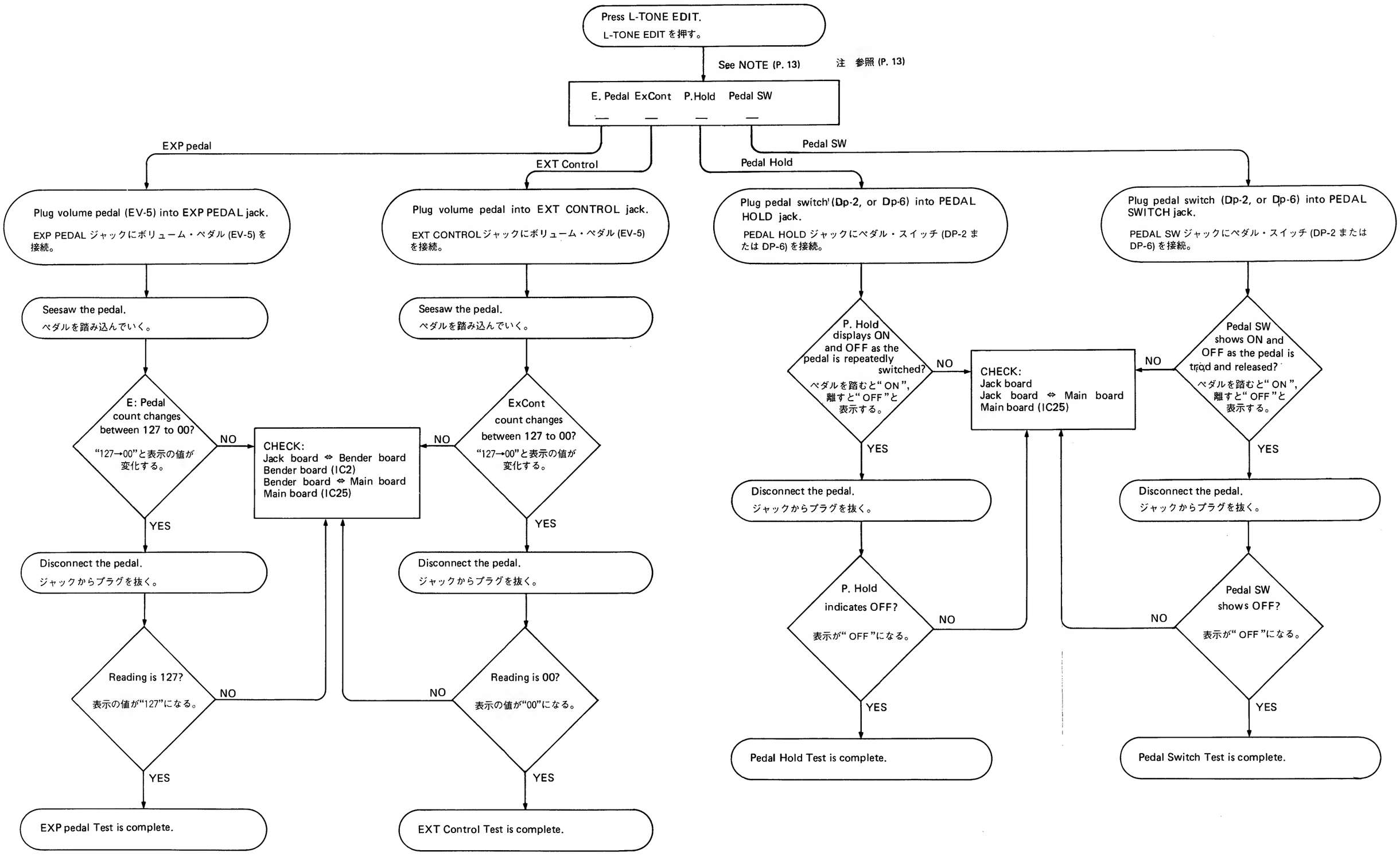
〔CONTROL TEST 1〕



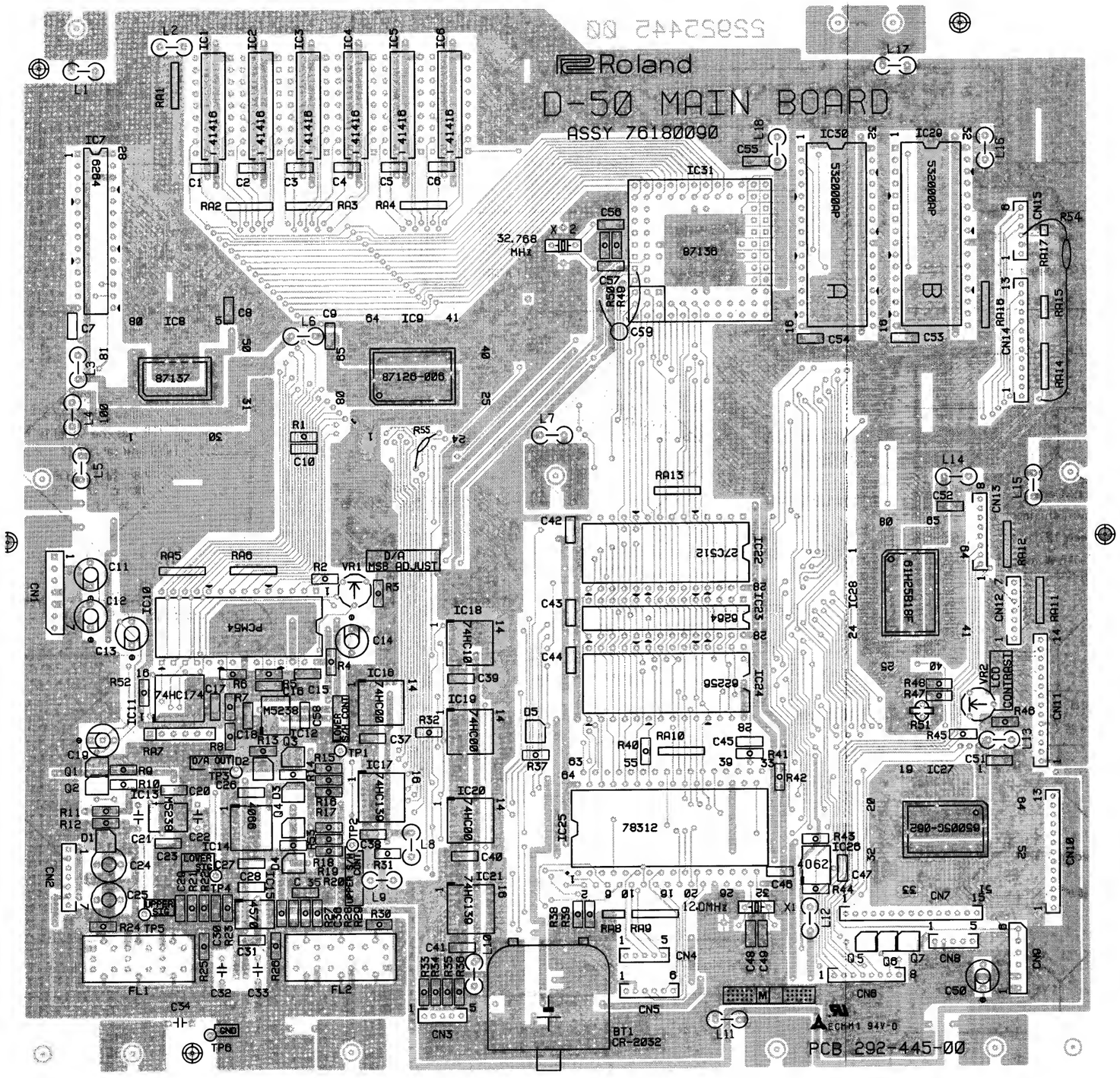
End of Control Test1.
Press EXIT and the display will return to the Test Menu.

コントロール・テスト 1 終了後は， EXIT を押してテスト・メニュー画面に戻す。

〔CONTROL TEST 2〕



MAIN BOARD 76180090 (pcb 22925445)



View from component side

ADVARSEL!

Lithiumbatteri. Eksplosionsfare.
Udskiftning må kun foretages af en sagkyndig, og som beskrevet i servicemanual.

Lithium batteri må kun udskiftes med samme type og fabrikat.

VARNING!

Lithiumbatteri. Explosionsrisk.
Får endast bytas av behörig servicetekniker.
Se instruktioner i servicemanualen.

Lithium batteri för endast ersättes med samme typ och fabrikat.

ADVARSEL!

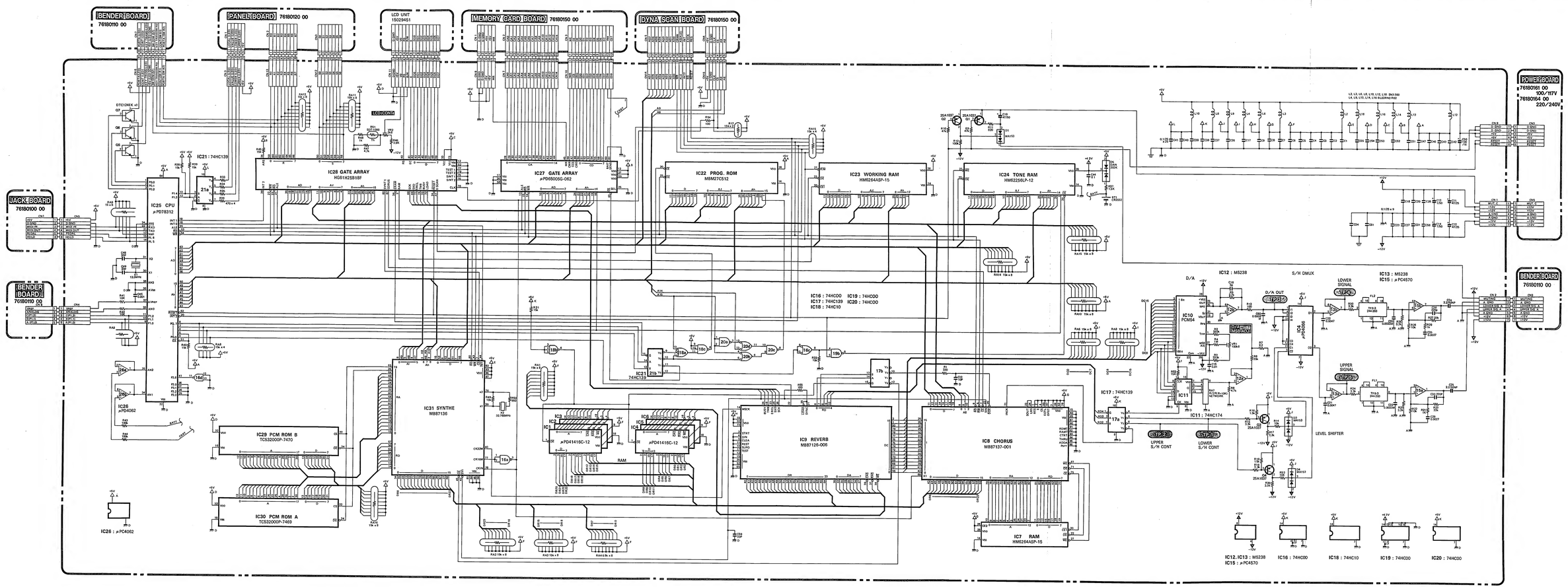
Lithiumbatteri. Fare for eksplotion.
Ma bare skiftes av kvalifisert tekniker som beskrevet i servicemanualen.

Lithium batteri må kun utskiftes med samme type og fabrikat.

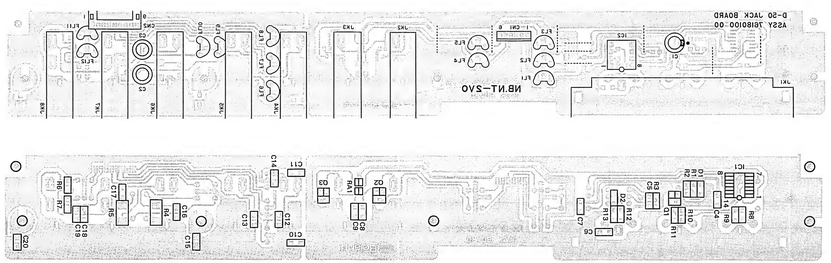
VAROITUS!

Lithiumparisto. Räjähdysvaara.
Pariston saa vaihtaa ainoastaan alan ammottimies.

Kun vaihat lithium pariston KÄYTÄ saman valmistajan samaa tyyppiä.

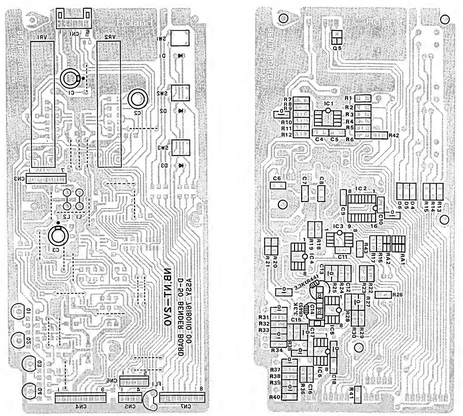

BENDER BOARD 76180110 00
PANEL BOARD 76180120 00
LCD UNIT 15029451
MEMORY CARD BOARD 76180150 00
DYNA SCAN BOARD 76180150 00
JACK BOARD 76180100 00
BENDER BOARD 76180110 00
POWER BOARD 76180161 00 100V/117V 76180164 00 220/240V
BENDER BOARD 76180110 00
IC25 CPU μPD78312
IC28 GATE ARRAY HG51N25B18F
IC27 GATE ARRAY μPD65005G-062
IC22 PROG. ROM M8M27C512
IC23 WORKING RAM HM6264ASP-15
IC24 TONE RAM HM62256LP-12
IC21 : 74HC139
IC16 : 74HC00 IC19 : 74HC00
IC17 : 74HC139 IC20 : 74HC00
IC18 : 74HC10
IC12 : M5238
IC13 : M5238
IC15 : μPC4570
D/A
S/H DMUX
D/A OUT
LOWER SIGNAL
UPPER SIGNAL
IC10 PCM54
IC4 μPD4066
IC11 : 74HC174
IC17 : 74HC139
UPPER S/H CONT
LOWER S/H CONT
LEVEL SHIFTER
IC26 μPD4062
IC31 SYNTHE M88T136
IC29 PCM ROM B TC532000P-7470
IC30 PCM ROM A TC532000P-7469
IC1 IC2 IC3 IC5 μPD41416C-12
RAM
IC9 REVERB M88T126-006
IC8 CHORUS M88T137-001
IC7 RAM HM6264ASP-15
IC26 : μPC4062
IC12,IC13 : M5238
IC15 : μPC4570
IC16 : 74HC00
IC18 : 74HC10
IC19 : 74HC00
IC20 : 74HC00

JACK BOARD 76180100 00 (pcb 22925446)

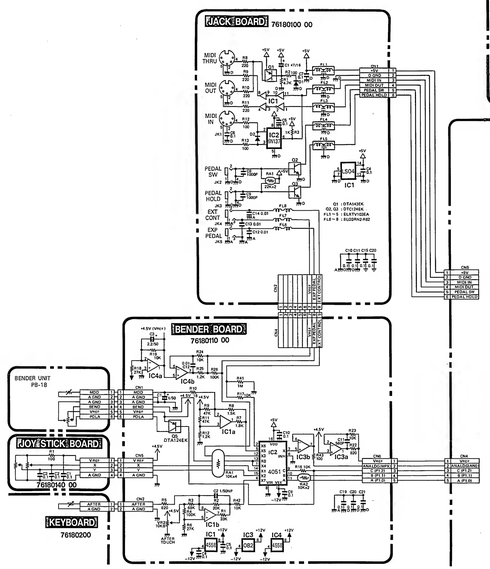


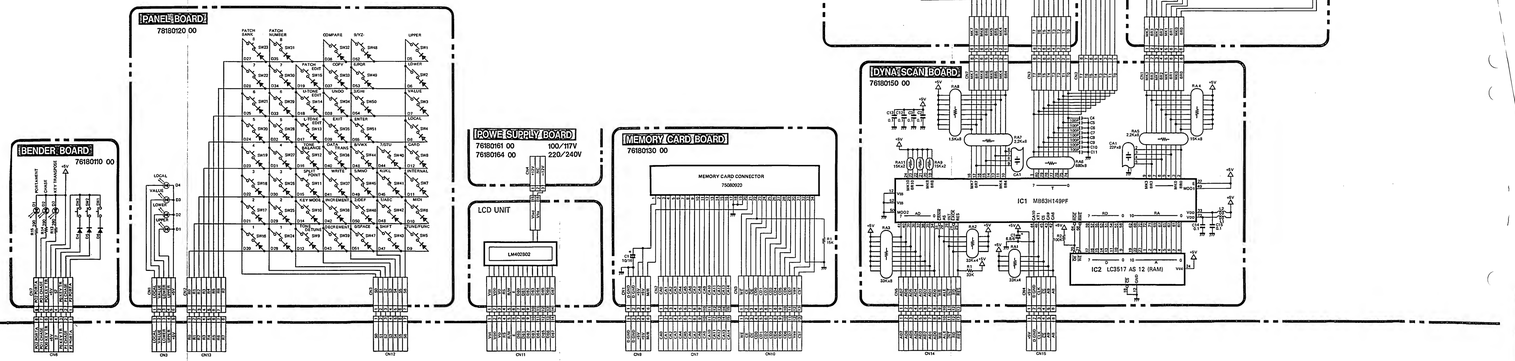
View from foil side

BENDER BOARD 76180110 (pcb 22925446)

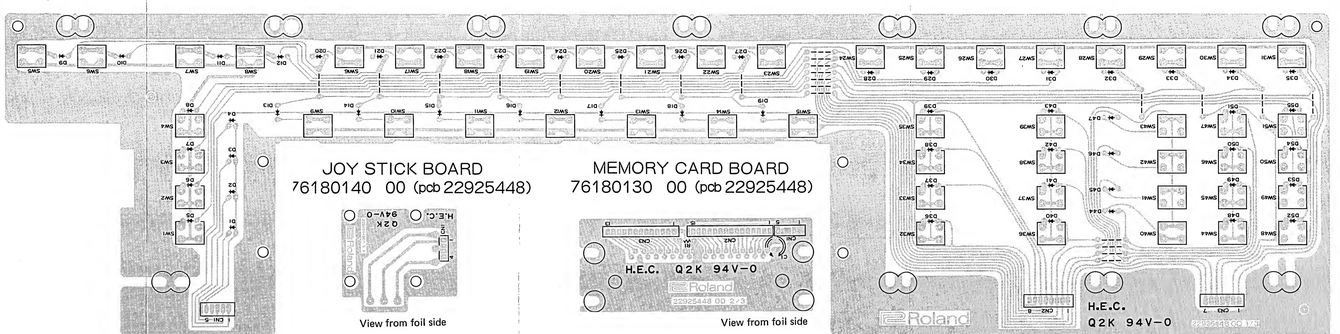


View from foil side





PANEL BOARD 76180120 00 (pcb 22925448)

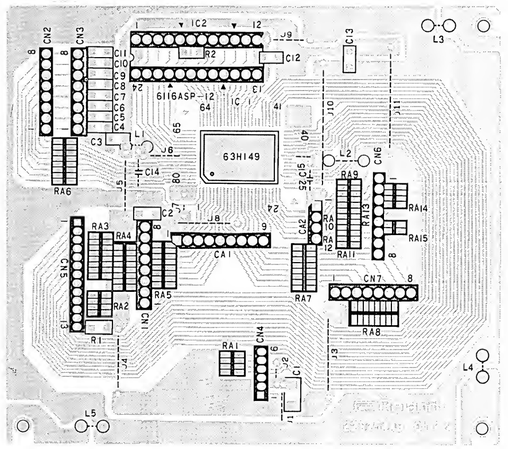


View from foil side

View from foil side

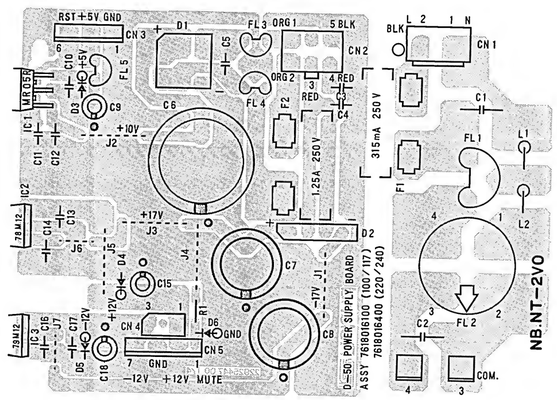
View from foil side

DYNA SCAN BOARD 76180150 00 (pcb 22925449)

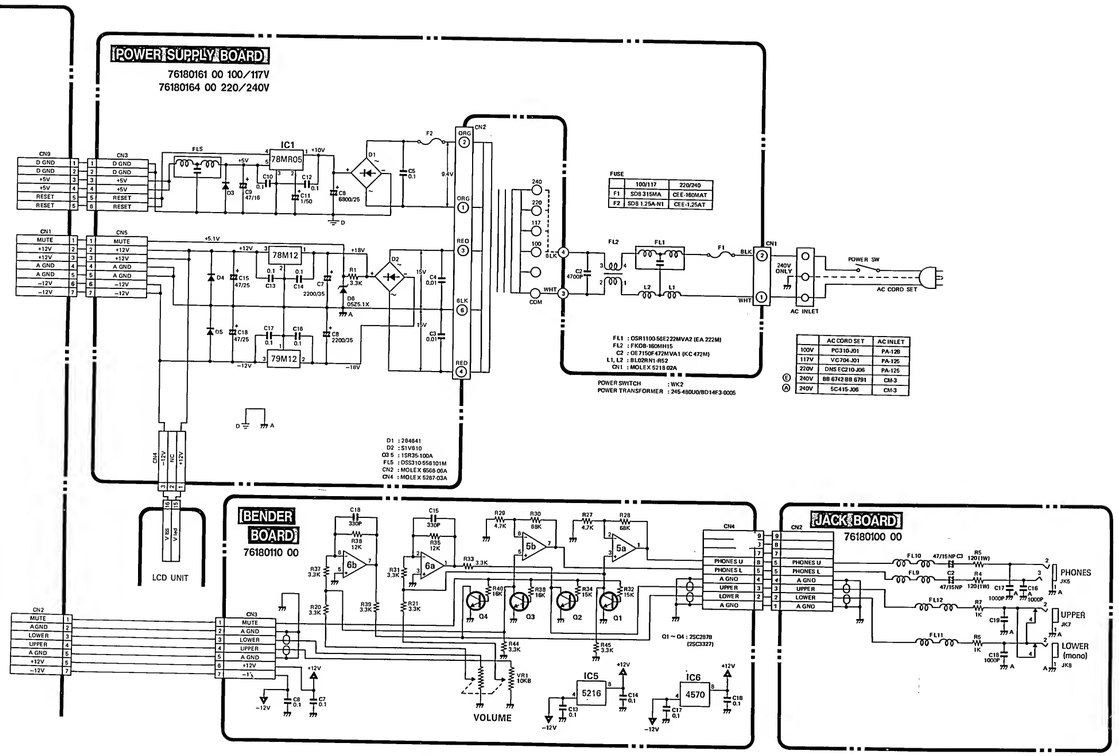


View from foil side

POWER SUPPLY BOARD 76180161 00 (100/117)
(pcb 22925447) 76180164 00 (220/240)



View from component side



8-16 VOICE DIGITAL KEYBOARD
MODEL D-50 **MIDI Implementation Chart**

Date : Feb. 07. 1987
Version : 1.00

Function...		Transmitted	Recognized	Remarks
Basic Channel	Default	1-16	1-16	Memorized
	Changed	1-16	1-16	
Mode	Default	Mode 3	Mode 1, 3, 4	Memorized
	Messages	POLY, OMNI OFF	MONO,POLY,OMNI ON/OFF	
	Altered	********	Mode 2 → Mode 1	
Note Number	True Voice	12-108	0-127	
		********	12-108	
Velocity	Note ON	○	○ v=1-127	
	Note OFF	× 9n v=0	×	
After Touch	Key's	×	×	
	Ch's	*	*	
Pitch Bender		*	* 0-12 semi	9 bit resolution
Control Change	1	*	*	Modulation
	5	*	*	Portamento Time
	7	*	*	Volume
	0-31	○	○ (0, 2-4, 8-31)	Ext Control
	6, 38	×	**	Data Entry (MSB, LSB)
	64	*	*	Hold 1
	65	*	*	Portamento SW
	64-95	○	○ (66-95)	Pedal Switch
	100, 101	×	** (0, 1)	RPC (LSB, MSB)
Prog Change	True #	* 0-127	* 0-127	
		********	0-127	
System Exclusive		*	*	
System common	Song Pos	×	×	
	Song scl	×	×	
	True	×	×	
System Real Time	Clock	×	×	
	Commands	×	×	
Aux Message	Local ON/OFF	×	○	Memorized
	All Notes OFF	○ (123)	○ (123-127)	
	Active Sense	×	○	
	Reset	×	×	
Notes		* Can be set to ○ or × manually, and memorized. ** RPC=Registered parameter control number. RPC#0 : Pitch bend sensitivity RPC#1 : Master fine tuning Parameter values are given by Data Entry.		

Mode 1 : OMNI ON, POLY
Mode 3 : OMNI OFF, POLY
Mode 2 : OMNI ON, MONO
Mode 4 : OMNI OFF, MONO
○ : Yes
× : No

MODEL D-50 **MIDI Implementation Chart** (Separate CH)

*Recognized if key mode in patch function is 'Sep' or 'Sep-S'.

Function...		Transmitted	Recognized	Remarks
Basic Channel	Default		1-16	Memorized
	Changed		1-16	
Mode	Default		Mode 3, 4 (M=1)	Memorized
	Messages		×	
	Altered	********		
Note Number	True Voice	********	0-127	
			12-108	
Velocity	Note ON		○ v=1-127	
	Note OFF		×	
After Touch	Key's		×	
	Ch's		*	
Pitch Bender			* 0-12 semi	9 bit resolution
Control Change	1		*	Modulation
	5		*	Portamento Time
	7		×	Volume
	0-31		○ (0, 2-4, 8-31)	Ext Control
	6, 38		**	Data Entry (MSB, LSB)
	64		*	Hold 1
	65		*	Portamento SW
	64-95		○ (66-95)	Pedal Switch
	100, 101		** (0)	RPC (LSB, MSB)
Prog Change	True #	********	×	
System Exclusive			×	
System common	Song Pos		×	
	Song sel		×	
	True		×	
System Real Time	Clock		×	
	Commands		×	
Aux Message	Local ON/OFF		○	Memorized
	All Notes OFF		○ (123)	
	Active Sense		○	
	Reset		×	
Notes		* Can be set to ○ or × manually, and memorized. ** RPC=Registered parameter control number. RPC#0 : Pitch bend sensitivity Parameter values are given by Data Entry.		

Mode 1 : OMNI ON, POLY
Mode 3 : OMNI OFF, POLY
Mode 2 : OMNI ON, MONO
Mode 4 : OMNI OFF, MONO
○ : Yes
× : No

8−16 VOICE DIGITAL KEYBOARD

MODEL D−50

MIDI Implementation

Date : Feb. 07. 1987

Version : 1.00

1. TRANSMITTED DATA

Status	Second	Third	Description	
1001 nnnn	0kkk kkkk	0000 0000	Note OFF kkkkkkk = 12 − 108	*1−1
1001 nnnn	0kkk kkkk	0vvv vvvv	Note ON kkkkkkk = 12 − 108 vvvvvvv = 1 − 127	
1011 nnnn	0000 0001	0vvv vvvv	Modulation depth vvvvvvv = 0 − 127	*1−2
1011 nnnn	0000 0111	0vvv vvvv	Main Volume vvvvvvv = 0 − 127	*1−2
1011 nnnn	000c cccc	0vvv vvvv	External control ccccc = 0 − 31 vvvvvvv = 0−127	*1−3
1011 nnnn	0100 0000	0000 0000	Hold1 OFF	*1−2, *1−4
1011 nnnn	0100 0000	0111 1111	Hold1 ON	*1−2
1011 nnnn	0100 0001	0000 0000	Portamento OFF	*1−2
1011 nnnn	0100 0001	0111 1111	Portamento ON	*1−2
1011 nnnn	0sss ssss	0000 0000	Pedal Switch OFF sssssss = 64 − 95	*1−5
1011 nnnn	0sss ssss	0111 1111	Pedal Switch ON sssssss = 64 − 95	*1−5
1100 nnnn	0ppp pppp		Program Change ppppppp = 0 − 127	*1−2, *1−6
1101 nnnn	0vvv vvvv		Channel After Touch vvvvvvv = 0 − 127	*1−2, *1−7
1110 nnnn	0vvv vvvv	0vvv vvvv	Pitch Bend Change	*1−2
1011 nnnn	0111 1011	0000 0000	All NOTES OFF	*1−1
1011 nnnn	0111 1100	0000 0000	OMNI OFF	*1−8
1011 nnnn	0111 1101	0000 0000	OMNI ON	*1−8
1111 0000	... ...	1111 0111	System exclusive	*1−9

Notes :

*1−1 Even if the transmit channel is changed while the keyboard is being played, data is transmitted on the previous transmit channel.

*1−2 Transmitted if the corresponding function switch is ON.

*1−3 'ccccc' can be selected by ExtCont in MIDI function.

*1−4 Even when the transmit channel is changed while Hold Pedal is being ON, data is transmitted on the previous transmit channel.

Transmitted even when Hold Function switch is turned to OFF while the Hold Pedal is being ON.

*1−5 'sssssss' can be selected by PedalSW in MIDI function.

*1−6 0 − 63 : Internal Memory Group
64 − 127 : Card Memory Group

*1−7 The maximum value is determined by the value of Aftertouch Volume.

*1−8 Transmitted at power−up.

When the transmit channel is changed, data is transmitted on the new channel.

*1−9 Transmitted on the channel set with BasicCH of MIDI Func, regardless of the transmit channel set in the patch.

See section 6 (TRANSMITTED EXCLUSIVE MESSAGES IN NOMAL MODE), section 7 (TRANSMITTED EXCLUSIVE MESSAGES IN DATA TRANSFER MODE).

2. RECOGNIZED RECEIVE DATA (MAIN CHANNEL)

Status	Second	Third	Description	
1000 nnnn	0kkk kkkk	0vvv vvvv	Note OFF,velocity ignored	*2−1
1001 nnnn	0kkk kkkk	0000 0000	Note OFF kkkkkkk = 12 − 108	*2−1
1001 nnnn	0kkk kkkk	0vvv vvvv	Note ON kkkkkkk = 12 − 108 vvvvvvv = 1 − 127	*2−1
1011 nnnn	0000 0001	0vvv vvvv	Modulation Depth vvvvvvv = 0 − 127	*2−2
1011 nnnn	0000 0101	0vvv vvvv	Portamento Time vvvvvvv = 0 − 127	*2−2
1011 nnnn	0000 0110	0vvv vvvv	Data Entry MSB	*2−3
1011 nnnn	0000 0111	0vvv vvvv	Main Volume vvvvvvv = 0 − 127	*2−2, *2−4
1011 nnnn	000c cccc	0vvv vvvv	External Control ccccc = 0, 2 − 4, 8 − 31 vvvvvvv = 0 − 127	*2−5
1011 nnnn	0010 0110	0vvv vvvv	Data Entry LSB	*2−3
1011 nnnn	0100 0000	0vvv vvvv	Hold1 OFF vvvvvvv = 0 − 63	*2−2
1011 nnnn	0100 0000	0vvv vvvv	Hold1 ON vvvvvvv = 64 − 127	*2−2
1011 nnnn	0100 0001	0vvv vvvv	Portamento OFF vvvvvvv = 0 − 63	*2−2
1011 nnnn	0100 0001	0vvv vvvv	Portamento ON vvvvvvv = 64 − 127	*2−2
1011 nnnn	0sss ssss	0vvv vvvv	Pedal Switch OFF sssssss = 66 − 95 vvvvvvv = 0 − 63	*2−6
1011 nnnn	0sss ssss	0vvv vvvv	Pedal Switch ON sssssss = 66 − 95 vvvvvvv = 64 − 127	*2−8
1011 nnnn	0110 0100	0vvv vvvv	RPC LSB	*2−3
1011 nnnn	0110 0101	0vvv vvvv	RPC MSB	*2−3
1100 nnnn	0ppp pppp		Program Change ppppppp = 0 − 127	*2−2, *2−7
1101 nnnn	0vvv vvvv		Channel After Touch vvvvvvv = 0 − 127	*2−2, *2−8
1110 nnnn	0vvv vvvv	0vvv vvvv	Pitch Bend Change	*2−2
1011 nnnn	0111 1010	0000 0000	Local OFF	*2−9
1011 nnnn	0111 1010	0111 1111	Local ON	*2−9
1011 nnnn	0111 1011	0000 0000	ALL NOTES OFF	*2−10
1011 nnnn	0111 1100	0000 0000	OMNI OFF	*2−10
1011 nnnn	0111 1101	0000 0000	OMNI ON	*2−10
1011 nnnn	0111 1110	000m mmmm	MONO ON	*2−10,*2−11
1011 nnnn	0111 1111	0000 0000	POLY ON	*2−10,*2−11
1111 0000	... ...	1111 0111	System exclusive	*2−12
1 1110			Active Sensing	

Notes :

*2−1 Note numbers outside the range 12 − 108 are transposed to the nearest octave inside this range.

*2−2 Recognized if the corresponding function switch is ON.

*2−3 RPC and value (Data Entry) are recognized as follows.

RPC#	value MSB	value LSB	Description
0	0vvv vvvv	0xxx xxxx	BEND RANGE (0−12 semitone, 1 semitone step) xxxxxxx is ignored.
1	0vvv vvvv	0vvv vvvv	MASTER TUNE (−50 − +50 cent)

*2−4 The volume of the snund can be controlled by main vnlume message within level which adjusted by the panel vnlume knob.

*2−5 'cccce' can be selected by ExtCont in MIDI function.

Recognized as fnlows depending on hnw the ExtCont mode nf Tune Func is set.

ExtCont mode	Function
'BAL'	Tone Balance
'AFTER'	Channel pressure
'MOD'	Moduration Depth
'OFF'	

*2−6 'ssssss' can be selected by PedalSW in MIDI function.

Recognized as folows depending on hnw the PedalSW mode nf Tune Func is set.

PedalSW mode	Function
'P−SFT'	Patch Shift
'PORTA'	Portamento ON/OFF
'CHASE'	Chase ON, OFF
'DFF'	

However, Patch Shift function is available only in Play mode. Also, Chase ON/OFF is recognized only when the key mode is Whole nr Dual.

*2−7 Recognized only in play mode.
0 − 63 : Internal Memory Group
64 − 127 : Card Memory Group

*2−8 Ignored if ExtCont in Tune/Func function is 'AFTER'.

*2−9 Ignored if key mode in patch function is 'Sep' or 'Sep−S'.

*2−10 Mode Messages (123 − 127) are also recognized as ALL NOTES OFF.

MONO channel range 'mmmmm' is recognized as follows.

mmmmm	True MONO channel range
0	8
1 − 8	1 − 8
9 − 16	8
17 − 127	ignore

In MONO mode, channel of recognized each message is as follows.

	Control in MIDI function	
Message	' B.CH '	' G.CH '
Note on/off	individual	individual
Control change	basic	global
Mode message	basic	basic
Program change	basic	global
Channel After Touch	basic	global
Pitch bend change	individual	individual
Exclusive	basic	basic

*Global channel is equal to "basic channel − 1".
And if basic channel is 1, global channel is 16.

*2−11 Ignored if Control in MIDI function is 'MdeOFF'.

*2−12 See section 6 (RECOGNIZED EXCLUSIVE MESSAGES IN NOMAL MODE), section 8 (RECOGNIZED EXCLUSIVE MESSAGES IN DATA TRANSFER MODE).

3. RECOGNIZED RECEIVE DATA (SEPARATE CHANNEL)

*Recognized if key mode in patch function is 'Sep' or 'Sep−S'.

Status	Second	Third	Description	
1000 nnnn	0kkk kkkk	0vvv vvvv	Note OFF,velocity ignored	*3−1
1001 nnnn	0kkk kkkk	0000 0000	Note OFF kkkkkkk=12 − 108	*3−1
1001 nnnn	0kkk kkkk	0vvv vvvv	Note ON kkkkkkk=12−108 vvvvvvv=1 − 127	*3−1
1011 nnnn	0000 0001	0vvv vvvv	Modulation depth vvvvvvv = 0 − 127	*3−2
1011 nnnn	0000 0101	0vvv vvvv	Portamento Time vvvvvvv = 0 − 127	*3−2
1011 nnnn	0000 0110	0vvv vvvv	Data Entry MSB	*3−3
1011 nnnn	000c cccc	0vvv vvvv	External Control ccccc = 0, 2 − 4, 8 − 31 vvvvvvv = 0 − 127	*3−4
1011 nnnn	0100 0000	0vvv vvvv	Hold1 OFF vvvvvvv = 0 − 63	*3−2
1011 nnnn	0100 0000	0vvv vvvv	Hold1 ON vvvvvvv = 64 − 127	*3−2
1011 nnnn	0100 0001	0vvv vvvv	Portamento OFF vvvvvvv = 0 − 63	*3−2
1011 nnnn	0100 0001	0vvv vvvv	Portamento ON vvvvvvv = 64 − 127	*3−2
1011 nnnn	0sss ssss	0vvv vvvv	Pedal Switch OFF sssssss = 66 − 95 vvvvvvv = 0 − 63	*3−5
1011 nnnn	0sss ssss	0vvv vvvv	Pedal Switch ON sssssss = 66 − 95 vvvvvvv = 64 − 127	*3−5
1011 nnnn	0110 0100	0vvv vvvv	RPC LSB	*3−3
1011 nnnn	0110 0101	0vvv vvvv	RPC MSB	*3−3
1101 nnnn	0vvv vvvv		Channel After Touch vvvvvvv = 0 − 127	*3−2, *3−6
1110 nnnn	0vvv vvvv	0vvv vvvv	Pitch Bend Change	*3−2
1011 nnnn	0111 1010	0000 0000	Local OFF	
1011 nnnn	0111 1010	0111 1111	Local ON	
1011 nnnn	0111 1011	0000 0000	ALL NOTES OFF	
1111 1110			Active Sensing	

Notes :

*3−1 Note numbers outside the range 12 − 108 are transposed to the nearest octave inside this range.

*3−2 Received if the corresponding function switch is ON.

*3−3 RPC and value (Data Entry) are recognized as follows.

RPC#	value MSB	value LSB	Description
0	0vvv vvvv	0xxx xxxx	BEND RANGE (0−12 semitone, 1 semitone step) xxxxxxx is ignored.

*3−4 'ccccc' can be selected by ExtCont in MIDI function.

Recognized as follows depending on the ExtCont mode of Tune/Func.

ExtCont Mode	Function
'BAL'	
'AFTER'	Channel pressure
'MOD'	Moduration Depth
'OFF'	

*3−5 'sssssss' can be selected by PedalSW in MIDI function.

Recognized as follows depending on the PedalSW mode of Tune/Func.

PedalSW Mode	Function
'P−SFT'	
'PORTA'	Portamento ON/OFF
'CHASE'	
'OFF'	

*3−6 Ignored if ExtCont in Tune/Func function is 'AFTER'.

4. EXCLUSIVE COMMUNICATION

4.1 Message structure

All exclusive communications are based on following structure
(Roland Exclusive Format Type IV).

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device−ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model−ID # (D−50)
e 0aaa aaaa	Command−ID #
[f 0bbb bbbb	Address MSB] [ ] depend on Command−ID
[g 0ccc cccc	Address]
[h 0ddd dddd	Address LSB]
[i 0eee eeee	Data]
[:	]
j 0fff ffff	Checksum
k 1111 0111	End of System Exclusive

Summed value of the all bytes between Command−ID and EOX (f−j) must be 00H (7 bits). It doesn't include Command−ID and EOX.

4.2 Address mapping

Address	Description		
Temporary area			
[00 − 00 − 00]	Upper Partial−1	temp.area	*4−1, *4−4
[00 − 00 − 40]	Upper Partial−2	temp.area	*4−1, *4−4
[00 − 01 − 00]	Upper Common	temp.area	*4−1, *4−5
[00 − 01 − 40]	Lower Partial−1	temp.area	*4−1, *4−4
[00 − 02 − 00]	Lower Partial−2	temp.area	*4−1, *4−4
[00 − 02 − 40]	Lower Common	temp.area	*4−1, *4−5
[00 − 03 − 00]	Patch	temp.area	*4−1, *4−6
Memory area			
[02 − 00 − 00]	Patch Memory	1−1	*4−2, *4−3
[02 − 03 − 40]	Patch Memory	1−2	*4−2, *4−3
:	:		
	Patch Memory	8−8	*4−2, *4−3
[03 − 00 − 00]	Reverb Data	17	*4−2, *4−7
[03 − 02 − 78]	Reverb Data	18	*4−2, *4−7
:	:		
[04 − 0C − 08]	Reverb Data	32	*4−2, *4−7

* [hh−mm−ll] 'hh', 'mm' and 'll' are showed by hex decimal.
0hhhhhhh 0mmmmmmm 0lllllll (binary), MS bit must be 0 .

Notes :

*4−1 Transmitted and recognized in NOMAL MODE.

*4−2 Transmitted and recognized in DATA TRANSFER MDDE.

*4−3 Each patch memory consists of the following.

Offset	Description	
[00 − 00 − 00]	Upper Partial−1	*4−4
[00 − 00 − 40]	Upper Partial−2	*4−4
[00 − 01 − 00]	Upper Common	*4−5
[00 − 01 − 40]	Lower Partial−1	*4−4
[00 − 02 − 00]	Lower Partial−2	*4−4
[00 − 02 − 40]	Lower Common	*4−5
[00 − 03 − 00]	Patch	*4−6

*4−4 Each partial block consists of the following.

Offset		Function	Value		
0	WG	Pitch Coarse	0 − 72	(C1,C#1 − C7)	
1	WG	Pitch Fine	0 − 100	(−50 − +50)	
2	WG	Pitch Keyfollow	0 − 16	(−1,−1/2,−1/4,0,1/8, 1/4,3/8,1/2,5/8,3/4, 7/8,1,5/4,3/2,2,s1, s2)	
3	WG	Mod LFO Mode	0 − 3	(OFF,(+),(−),A&L)	
4	WG	Mod P−ENV Mode	0 − 2	(OFF,(+),(−)	
5	WG	Mod Bend Mode	0 − 2	(OFF,Keyfollow,Normal)	
6	WG	Wave Form	0 − 1	(Squsre,Sawtooth)	
7	WG	PCM Wave No.	0 − 99	(1 − 100)	
8	WG	Pulse Width	0 − 100		
9	WG	PW Velocity Range	0 − 14	(−7 − +7)	
10	WG	PW LFO Select	0 − 5	(+1,−1,+2,−2,+3,−3)	
11	WG	PW LFO Depth	0 − 100		
12	WG	PW After touch Range	0 − 14	(−7 − +7)	
13	TVF	Cutoff Frequency	0 − 100		
14	TVF	Resonance	0 − 30		
15	TVF	Keyfollow	0 − 14	(−1,−1/2,−1/4,0,1/8, 1/4,3/8,1/2,5/8,3/4, 7/8,1,5/4,3/2,2)	
16	TVF	Bias Point/Dir	0 − 127	(<A1−<C7,>A1−>C7)	
17	TVF	Bias Level	0 − 14	(−7 − +7)	
18	TVF ENV	Depth	0 − 100		
19	TVF ENV	Velocity Range	0 − 100		
20	TVF ENV	Depth Keyfollow	0 − 4		
21	TVF ENV	Time Keyfollow	0 − 4		
22	TVF ENV	Time 1	0 − 100		
23	TVF ENV	Time 2	0 − 100		
24	TVF ENV	Time 3	0 − 100		
25	TVF ENV	Time 4	0 − 100		
26	TVF ENV	Time 5	0 − 100		
27	TVF ENV	Level 1	0 − 100		
28	TVF ENV	Level 2	0 − 100		
29	TVF ENV	Level 3	0 − 100		
30	TVF ENV	Sustain Level	0 − 100		
31	TVF ENV	End Level	0 − 1	(0,100)	
32	TVF Mod	LFOSelect	0 − 5	(+1,−1,+2,−2,+3,−3)	
33	TVF Mod	LFO Depth	0 − 100		
34	TVF Mod	After touch Range	0 − 14	(−7 − +7)	
35	TVA	Level	0 − 100		
36	TVA	Velocity Range	0 − 100	(−50 − +60)	
37	TVA	Bias Point	0 − 127	(<A1−<C7,>A1−>C7)	
38	TVA	Bias Level	0 − 12	(−12 − 0)	
39	TVA ENV	Time 1	0 − 100		
40	TVA ENV	Time 2	0 − 100		
41	TVA ENV	Time 3	0 − 100		
42	TVA ENV	Time 4	0 − 100		
43	TVA ENV	Time 5	0 − 100		
44	TVA ENV	Level 1	0 − 100		
45	TVA ENV	Level 2	0 − 100		
46	TVA ENV	Level 3	0 − 100		
47	TVA ENV	Sustain Level	0 − 100		
48	TVA ENV	End Level	0 − 1	(0,100)	
49	TVA ENV	Velocity Follow	0 − 4		
50	TVA ENV	Time Keyfollow	0 − 4		
51	TVA Mod	LFO Select	0 − 5	(+1, −1,+2,−2,+3,−3)	
52	TVA Mod	LFO Depth	0 − 100		
53	TVA Mod	After touch Range	0 − 14	(7 − 7)	
54	Extension	(for future)	0		
55	Extension		0		
56	Extension		0		
57	Extension		0		
58	Extension		0		
59	Extension		0		
60	Extension		0		
61	Extension		0		
62	Extension		0		
63	Extension		0		

*4−5 Each common block consists of the following.

Offset	Function	Value	
0	Tone Name 1	0 − 63	(' ','A'−'Z','a'−'z', '1'−'9','0','−')
1	Tone Name 2	0 − 63	...
2	Tone Name 3	0 − 63	...
3	Tone Name 4	0 − 63	...
4	Tone Name 5	0 − 63	...
5	Tone Name 6	0 − 63	...
6	Tone Name 7	0 − 63	...
7	Tone Name 8	0 − 63	...
8	Tone Name 9	0 − 63	...
9	Tone Name 10	0 − 63	...
10	Structure No.	0 − 6	(1 − 7)
11	P−ENV Velocity Range	0 − 2	
12	P−ENV Time Keyfollow	0 − 4	
13	P−ENV Time 1	0 − 50	
14	P−ENV Time 2	0 − 50	
15	P−ENV Time 3	0 − 50	
16	P−ENV Time 4	0 − 50	
17	P−ENV Level 0	0 − 100	(−50 − +50)
18	P−ENV Level 1	0 − 100	(−50 − +50)
19	P−ENV Level 2	0 − 100	(−50 − +50)
20	P−ENV Sustain Level	0 − 100	(−50 − +50)
21	P−ENV End Level	0 − 100	(−50 − +50)
22	P−Mod LFO Depth	0 − 100	
23	P−Mod Lever	0 − 100	
24	P−Mod After touch	0 − 100	
25	LFO−1 Wave Form	0 − 3	(TRI,SAW,SQU,RND)
26	LFO−1 Rate	0 − 100	
27	LFO−1 Delay Time	0 − 100	
28	LFO−1 Sync	0 − 2	(OFF,ON,KEY)
29	LFO−2 Wave Form	0 − 3	(TRI,SAW,SQU,RND)
30	LFO−2 Rate	0 − 100	
31	LFO−2 Delay Time	0 − 100	
32	LFO−2 Sync	0 − 1	(OFF,ON)
33	LFO−3 Wave Form	0 − 3	(TRI,SAW,SQU,RND)
34	LFO−3 Rate	0 − 100	
35	LFO−3 Delay Time	0 − 100	
36	LFO−3 Sync	0 − 1	(OFF,ON)
37	Low EQ Frequency	0 − 15	(63, 75, 88,105,125, 150,176,210,260,300, 360,420,500,600,700, 840)
38	Low EQ Gain	0 − 24	(−12 − +12)
39	Low EQ Frequency	0 − 21	(260,300,350,420,600, 600,700,840,1.0,1.2, 1.4,1.7,2.0,2.4,2.8, 3.4,4.0,4.8,5.7,6.7, 8.0,9.5)
40	High EQ Q	0 − 8	(0.3,0.6,0.7,1.0,1.4, 2.0,3.0,4.2,6.0)
41	High EQ Gain	0 − 24	(−12 − +12)
42	Chorus Type	0 − 7	(1 − 8)
43	Chorus Rate	0 − 100	
44	Chorus Depth	0 − 100	
45	Chorus Balance	0 − 100	
46	Partial Mute	0 − 3	(00,01,10,11)
47	Partial Balance	0 − 100	
48	Extension (for future)	0	
49	Extension	0	
50	Extension	0	
51	Extension	0	
52	Extension	0	
53	Extension	0	
54	Extension	0	
55	Extension	0	
56	Extension	0	
57	Extension	0	
58	Extension	0	
59	Extension	0	
60	Extension	0	
61	Extension	0	
62	Extension	0	
63	Extension	0	

8.2.2 Request data RQD1 41H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0100 0001	Command-ID # (RQD1)
f 0000 0010	Address MSB *8-1
g 0000 0000	Address
h 0000 0000	Address LSB
i 0ddd dddd	Size MSB *8-3
j 0eee eeee	Size
k 0fff ffff	Size LSB
l 0ggg gggg	Checksum
m 1111 0111	End of System Exclusive

8.2.3 Data set DAT 42H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0100 0010	Command-ID # (DAT)
f 0aaa aaaa	Address MSB *8-1
g 0bbb bbbb	Address
h 0ccc cccc	Address LSB
i 0ddd dddd	Data *8-2
:	
j 0eee eeee	Checksum
k 1111 0111	End of System Exclusiva

8.2.4 Acknowledge ACK 43H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channal #
d 0001 0100	Model-ID # (D-50)
e 0100 0011	Command-ID # (ACK)
f 1111 0111	End of System Exclusive

8.2.5 End of data EOD 46H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0100 0101	Command-ID # (EOD)
f 1111 0111	End of System Exclusive

8.2.6 Communication error ERR 4EH

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0100 1110	Command-ID # (ERR)
f 1111 0111	End of System Exclusive

8.2.7 Rejection RJC 4FH

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0100 1111	Command-ID # (RJC)
f 1111 0111	End of System Exclusive

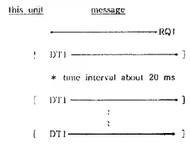
Notes :
*8-1 If the assinged address exceeds Memory area, it is ignores,

*8-2 Number of data in data set (DT1, DAT) should not exceed 266,

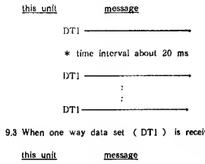
*8-3 The size that exceeds Memory area should not be assinged,

9. Sequence of communication

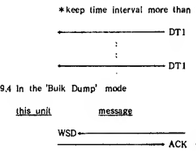
9.1 When one way request data (RQ1) is received



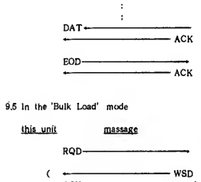
9.2 When one way data set (DT1) is transmitted



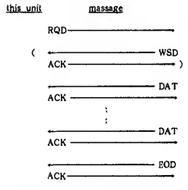
9.3 When one way data set (DT1) is received



9.4 In the 'Bulk Dump' mode



9.5 In the 'Bulk Load' mode



Notes :
*It sends RJC and stops the sequence when it receives ERR or detects some error.

*It sends RJC when the sequence is discontinued manually.

*It stops the sequence immediately when it receives RJC.

7. TRANSMITTED EXCLUSIVE MESSAGES IN DATA TRANSFER MODE

7.1 One way transfer

7.1.1 Data set DT1 12H

Transmitted when 'ENTER' button is pressed in 'Bulk Dump.O' mode.

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland tD #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0001 0010	Command-ID # (DT1)
f 0aaa aaaa	Address MSB *7-1
g 0bbb bbbb	Address
h 0ccc cccc	Address LSB
i 0ddd dddd	Data *7-2
:	
j 0eee eeee	Checksum
k 1111 0111	End of System Exclusive

7.2 Handshaking communication

7.2.1 Want to send data WSD 40H

Transmitted when 'ENTER' button is pressed in 'Bulk Dump' mode.

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0100 0000	Command-ID # (WSD)
f 0000 0010	Address MSB *7-1
g 0000 0000	Address
h 0000 0000	Address LSB
i 0000 0010	Size MSB *7-3
j 0000 1111	Size
k 0000 0000	Size LSB
l 0110 1101	Checksum
m 1111 0111	End of System Exclusive

7.2.3 Data set DAT 42H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0100 0010	Command-ID # (DAT)
f 0aaa aaaa	Address MSB *7-1
g 0bbb bbbb	Address
h 0ccc cccc	Address LSB
i 0ddd dddd	Data *7 2
:	
j 0eee eeee	Checksum
k 1111 0111	End of System Exclusive

7.2.4 Acknowledge ACK 43H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0001 0011	Command-ID # (ACK)
f 1111 0111	End of System Exclusive

7.2.5 End of data EOD 45H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0100 0101	Command-ID # (EOD)
f 1111 0111	End of System Exclusive

7.2.6 Rejection RJC 4FH

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0100 1111	Command-ID # (RJC)
f 1111 0111	End of System Exclusive

Notes :
*7-1 Address of first Data set command (DT1, DAT), Want to send date (WSD) or Request data (RQD) is [02-00-00] top of memory area.

*7-2 Number nf data in data set (DT1, DAT) sould not exceed 256.

*7-3 Number of memory data (including reverb 17 - 32).

8. RECOGNIZED EXCLUSIVE MESSAGES IN DATA TRANSFER MODE

8.1 One way transfer

8.1.1 Data set DT1 12H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0001 0010	Command-ID # (DT1)
f 0aaa aaaa	Address MSB *8-1
g 0bbb bbbb	Address
h 0ccc cccc	Address LSB
i 0ddd dddd	Data *8-2
:	
j 0eee eeee	Checksum
k 1111 0111	End of System Exclusive

8.2 Handshaking communication

8.2.1 Want to send data WSD 40H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0100 0000	Command-ID # (WSD)
f 0aaa aaaa	Address MSB *8-1
g 0bbb bbbb	Address
h 0ccc cccc	Address LSB
i 0ddd dddd	Size MSB *8-3
j 0eee eeee	Siza
k 0fff ffff	Size LSB
l 0ggg gggg	Checksum
m 1111 0111	End of System Exclusive

*4-6 Each patch block consists of the following.

Offset	Funetion	Value	
0	Patch Name 1	0 - 63	(' ','A'-'Z','a'-'z', '1'-'9','0',' -')
1	Patch Name 2	0 - 63	...
2	Patch Name 3	0 - 63	...
3	Patch Name 4	0 - 63	...
4	Patch Name 5	0 - 63	...
5	Patch Name 6	0 - 63	...
6	Patch Name 7	0 - 63	...
7	Patch Name 8	0 - 63	...
8	Patch Name 9	0 - 63	...
9	Patch Name 10	0 - 63	...
10	Patch Name 11	0 - 63	...
11	Patch Name 12	0 - 63	...
12	Patch Name 13	0 - 63	...
13	Patch Name 14	0 - 63	...
14	Patch Name 15	0 - 63	...
15	Patch Name 16	0 - 63	...
16	Patch Name 17	0 - 63	...
17	Patch Name 18	0 - 63	...
18	Key Mode	0 - 8	(Whole,Dual,Split, Separate,Whole-S, Dual-S,Split-US, Split-LS,Separate-S)
19	Split Point	0 - 60	(C2,C#2 - C7)
20	Portamento Mode	0 - 2	(U,L,UL)
21	Hold Mode	0 - 2	(U,L,UL)
22	Upper Tone Key Shift	0 - 48	(-24 - +24)
23	Lower Tone Key Shift	0 - 48	(-24 - +24)
24	Upper Tone Fine Tune	0 - 100	(-50 - +50)
25	Lower Tone Fine Tuna	0 - 100	(-50 - +50)
26	Bender Range	0 - 12	
27	After touch Bend Range	0 - 24	(-12 - +12)
28	Portamento Time	0 - 100	
29	Output Mode	0 - 3	(1 - 4)
30	Reverb Type	0 - 31	(1 - 32)
31	Reverb Balance	0 - 100	
32	Total Volume	0 - 100	
33	Tone Balence	0 - 100	
34	Chase Mode	0 - 2	(UL,ULL,ULU)
35	Chase Level	0 - 100	
36	Chase Time	0 - 100	
37	MIDI Transmit Channel	0 - 15	(Basic CH, 1 - 16)
38	MIDI Separate Rcv Channel	0 - 16	(OFF,1 - 16)
39	Extension (for futura)	0	
40	Extension	0	
41	Extension	0	
42	Extension	0	
43	Extension	0	
44	Extension	0	
45	Extension	0	
46	Extension	0	
47	Extension	0	
48	Extension	0	
49	Extension	0	
50	Extension	0	
51	Extension	0	
52	Extension	0	
53	Extension	0	
54	Extension	0	
55	Extension	0	
56	Extension	0	
57	Extension	0	
58	Extension	0	
59	Extension	0	
60	Extension	0	
61	Extension	0	
62	Extension	0	
63	Extension	0	

*4-7 Each reverb block (17 - 32) consists of the following.

000000	0000 aaaa	Reverb data 1	
	0000 aaaa		
2	0000 aaaa	Reverb data 2	
	0000 aaaa		
	:		
374	0000 aaaa	Reverb data 188	
	0000 aaaa		

5. TRANSMITTED EXCLUSIVE MESSAGES IN NORMAL MODE

5.1 Data set (One way) DT1 121t

Transmitted only when 'Request data (RQ1)' is recognized.

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0001 0001	Command-ID # (RQ1)
f 0aaa aaaa	Address MSB *5-1
g 0bbb bbbb	Address
h 0ccc cccc	Address LSB
i 0ddd dddd	Size MSB *6-1
j 0eee eeee	Size
k 0fff ffff	Size LSB
l 0ggg gggg	Checksum
m 1111 0111	End of System Exclusive

6.2 Date set (Ona way) DT1 12H

Recngnized if Exclu in tha MIDI function is on.

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0001 0010	Command-ID # (DT1)
f 0aaa aaaa	Address MSB *6-1
g 0bbb bbbb	Address
h 0ccc cccc	Address LSB
i 0ddd dddd	Data *6-2
:	
j 0eae eeee	Checksum
k 1111 0111	End of System Exclusive

Notes :
*5-1 Transmitted several times in smaller portion than the total number 256 in data byte of each message accroding to the address size assinged with Request Data (RQ1).

6. RECOGNIZED EXCLUSIVE MESSAGES IN NOMAL MODE

6.1 Request Data (One way) RQ1 11H

Recognized if Exclu in the MIDI function is on.

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #
d 0001 0100	Model-ID # (D-50)
e 0001 0001	Command-ID # (RQ1)
f 0aaa aaaa	Address MSB *6-1
g 0bbb bbbb	Address
h 0ccc cccc	Address LSB
i 0ddd dddd	Size MSB *6-1
j 0eee eeee	Size
k 0fff ffff	Size LSB
l 0ggg gggg	Checksum
m 1111 0111	End of System Exclusive

Notes :
*6-1 Any address size can be assinged within the range of Temp.area.

*6 2 Number of the data bytes should not exceed 256, (except sum)